

Development of next-generation system-on-package (SOP) technology based on silicon carriers with fine-pitch chip interconnection

System-on-Package (SOP) technology based on silicon carriers has the potential to provide modular design flexibility and high-performance integration of heterogeneous chip technologies and to support robust chip manufacturing with high-yield/low-cost chips for a wide range of two- and three-dimensional product applications. Key technology enablers include silicon through-vias, high-density wiring, high-I/O chip interconnection, and supporting test and assembly technologies. The silicon through-vias are a key feature permitting efficient area array signal, power, and ground interconnection through these thinned silicon packages. High-density wiring and high-density chip I/O interconnection can enable tight integration of heterogeneous chip technologies which approximate the performance of an integrated system-on-chip with a “virtual chip” using the silicon package for integration. Silicon carrier fabrication leverages existing manufacturing capability and mid-UV lithography to provide very dense package wiring following CMOS back-end-of-line design rules. Further, the thermal expansion of the silicon carrier package matches the chip, which helps maintain reliability even as the high-density chip microbump interconnections scale to smaller size. In addition to heterogeneous chip integration, SOP products may leverage the integration of passive components, active devices, and electro-optic structures to enhance system-level performance while also maintaining functional test capability and known good chips when needed. This paper describes the technical challenges and recent progress made in the development of silicon carrier technology for potential new applications.

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Introduction

Over the past 30 years, IBM has provided leadership in packaging technology with the introduction of multichip modules (MCMs) in the 1970s, thermal conduction modules (TCMs) in the 1980s and 1990s, and advanced organic micro-via buildup-layer technology in the 1990s and 2000s [1–9]. Silicon-based packaging (SBP) can potentially affect packaging technology in the near future. Next-generation products can utilize silicon carriers with silicon through-vias, high wiring density, and fine-pitch

interconnections; they can leverage advanced cooling technology and new test capabilities, and can support two- and three-dimensional structures. Advanced semiconductor circuit designs can contain more than 100 million circuits with interconnection densities in the range of 10^6 to 10^8 cm^{-2} . Consequently, products with the lowest cost, smallest size, and best performance have often utilized system-on-chip (SOC) product solutions in which the system functions can be manufactured on a single wafer using compatible semiconductor processes [10].

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For many product applications, system complexity and manufacturing process integration needs do not permit a solution on one chip; instead, heterogeneous semiconductor technologies are required. Where very-high-I/O interconnections are needed to interconnect these heterogeneous semiconductor technologies and for applications which require miniaturization, traditional packaging technologies such as ceramic or organic chip carriers may not support the I/O interconnection level needs. New packaging approaches, such as silicon through-via chip stacks and packages, may begin to complement or replace traditional interconnection and packaging, such as advanced wire-bond chip stack packages and ceramic or organic chip carriers. A silicon carrier with silicon through-vias and high-density wiring provides a means of tightly integrating different chip technologies and achieving SOC performance with a new "virtual chip" or SOP solution.

The goals of an SOP technology based on silicon carrier technology are 1) to provide modular chip design flexibility; 2) to integrate heterogeneous technologies with performance comparable to or exceeding that of single-chip integration; 3) to support high chip manufacturing yield; and 4) to deliver low-cost products. With a silicon carrier, each chip can be individually optimized for system performance and manufacturing yield. Packaging based on silicon through-vias can provide the foundation for new SOP products with electro-optic technology [11, 12], and silicon-based mini-multichip modules (MMCMs) are attractive for both commodity and complex product applications.

SBP solutions for package interconnection and wiring have been proposed at times over the past 30 years, beginning with a proposed silicon package in 1972 [13]. However, such approaches have utilized perimeter connections for a chip or silicon package, and perimeter connections are often inadequate because of power distribution and signal I/O limitations. Silicon-based packaging can provide very dense wiring using back-end-of-line (BEOL) processing. The BEOL wiring ground rules can be those of previous silicon generations, enabling high-yield and low-cost fabrication. The thermal expansion of the silicon carrier is identical to that of the silicon devices mounted on it, increasing the chip-package interface reliability. Matched thermal expansion also allows the use of advanced interconnections such as solder microbumps [controlled collapse chip connection (reworkable) microbumps (μ -C4s)], or (permanent) copper interconnections between the chips and the silicon carrier. Furthermore, this technology offers the possibility of embedding active devices in the carrier itself, such as DRAM for cache memory, phase-locked loops, or I/O drivers. Silicon carriers with through-vias can support heterogeneous semiconductor technologies, provide

passive or active circuits and high-density I/O wiring interconnections with electro-optic technology, and support three-dimensional circuit integration. SOP silicon-carrier technology can provide both high-performance and low-cost packaging solutions, extendible with advances in semiconductor lithography.

Figure 1 illustrates some projected trends for three areas within the packaging technology: 1) thermal cooling, 2) first-level interconnections and packaging, and 3) second-level interconnections and printed wiring boards (PWBs). Advances in interface materials for thermal cooling will increase the capacity for direct heat conduction from 50 W-cm⁻² to 90–120 W-cm⁻². Additional cooling can be achieved with liquid as micro-channel liquid cooling, or with jet impingement of liquids, thus reducing the chip operating temperature. Since chip performance increases with decreasing operating temperature, liquid cooling provides an opportunity to optimize the chip design for balancing performance and cooling capacity. First-level interconnection technology, such as flip-chip technology, continues to progress toward finer I/O pitch and wiring, based primarily on organic and ceramic packaging solutions. Emerging solutions such as chip stacking and the use of silicon for packaging should support even higher levels of integration. Even higher chip integration can be achieved through 3D chip wiring. However, to benefit from this increasing integration capability, precision alignment with cost-effective assembly and testing must be achieved at a reliability suitable for the targeted applications. Improvements in second-level interconnection and enhanced printed wiring boards (PWBs) are needed in order to support higher communication frequencies by combining electrical and optical interconnections. Optical integration can provide increased communication bandwidth at lower power and longer distances than electrical wiring. For short distances, however, it is expected that electrical integration will continue to be utilized at ever-higher frequencies and in cost-effective ways until optical integration becomes available at lower costs or becomes practical because of space constraints.

Figure 2 illustrates some projected future 2D and 3D package and chip integration approaches with increasing levels of integration. Approaches utilizing a silicon chip stack, silicon carrier, or three-dimensional chip circuits offer benefits such as modular design, improved performance, and lower manufacturing cost. For any new packaging technology, assembly, test, and reliability must be cost-effective in order to take advantage of increased integration capability and performance. For silicon chip stacks, the use of silicon through-vias provides a higher I/O count than perimeter connections. Compared with wire-bond chip stack technology, through-silicon vias also have shorter interconnection distances between

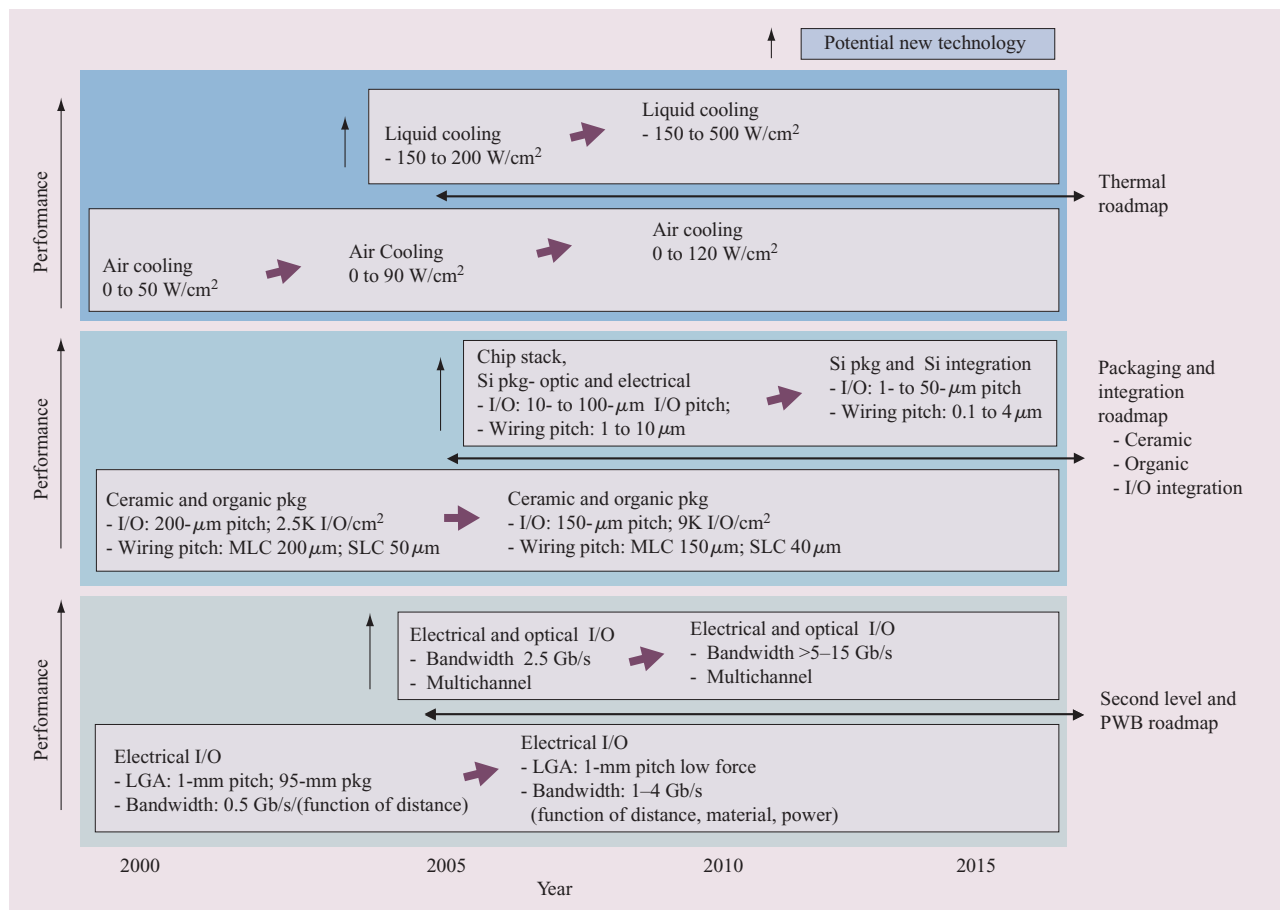


Figure 1

Packaging technology roadmap showing thermal, interconnect, packaging, and printed wiring board (PWB) trends. (LGA = land grid array; SLC = surface laminar circuit = organic packaging; MLC = multilayer ceramic.)

circuits, with lower electrical parasitic losses, supporting higher-frequency operation. Silicon carrier MMCMs offer great flexibility to integrate electrical and optical components. Besides conductive through-via wiring, silicon carriers can include integrated passive devices, microelectrical-mechanical systems (MEMs), and micromachined recesses for self-aligned assembly of optical components. In addition, fine-pitch μ -C4 connection pads on the top side of the silicon carrier allow a very high density of interconnections between flip-chip-mounted components. The chip-to-chip spacing, inter-chip wiring, and I/O densities can be improved by a factor of 10 $\times$ to 100 $\times$ compared with current packaging capabilities, supporting the integration of high-performance heterogeneous technologies. Since the silicon carrier has a thermal coefficient of expansion identical to that of silicon chips, it is expected that interconnection pitches may measure a few tens of

microns or less for solder interconnections and may be much smaller for copper interconnections. For three-dimensional circuit integration using stacked-wafer structures, continuing advances in wafer-level processing and integration may provide even shorter net lengths for applications by leveraging wiring in three dimensions.

Figure 3 shows schematic cross sections of (a) an integrated chip stack/interposer, (b) an opto-electronic transceiver, and (c) an MMCM, with representative photographs of silicon-based packaging applications.

This paper reports recent progress in the development of SBP technology with silicon through-via packages, opportunities for chip stack, silicon-based electro-optical packaging, and MMCM package integration. Discussion includes industry advances in the field, design considerations, and theoretical and experimental results; and the technical challenges for fabrication of silicon through-via conductors are highlighted.

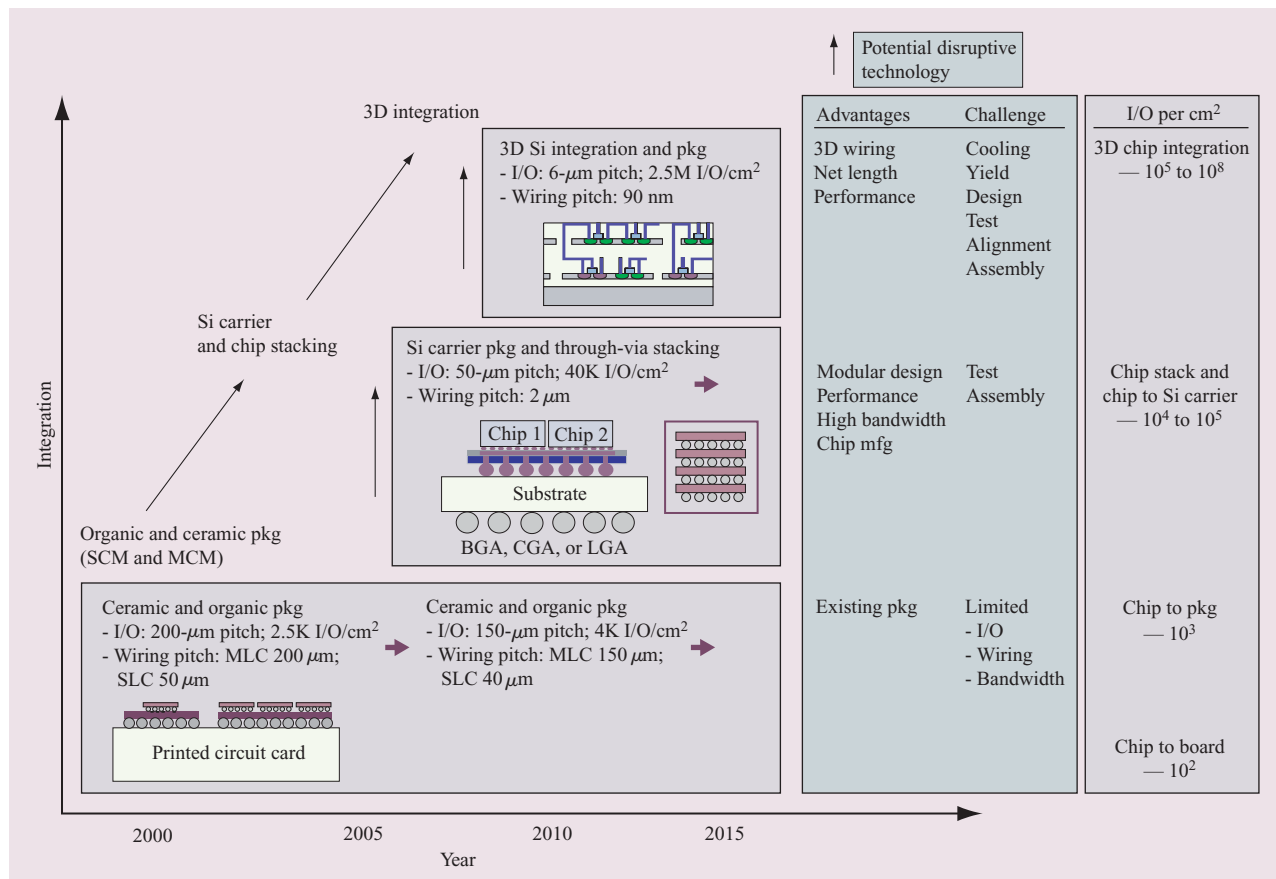


Figure 2

Silicon integration roadmap showing ceramic and organic area array integration, silicon carrier and chip stack integration, and circuit-level 3D integration. (SCM = single-chip module; MCM = multichip module; LGA = land grid array; BGA = ball grid array; CGA = column grid array; MLC = multilayer ceramic; SLC = surface laminar circuit.)

Industry advances in chip stacking and integration

In 1972, silicon-on-silicon structures were reported by D. J. Bodendorf et al. [13] in which passive or active silicon carriers with attached C4s were proposed. One proposed benefit was the matched coefficient of thermal expansion between the chips and the carrier to address thermal-cycle fatigue concerns for interconnections. Since then, industry utilization of chip-on-chip stacking has taken a variety of form factors such as the use of wire bonding and system integration of very-large-scale-integration (VLSI) semiconductor chips. The expansion of integration has been significant, especially from the 1990s to the present. In the early 1990s, examples of chip stack technology began with two chips stacked with adhesive and wire-bonded at the chip perimeter. In the mid-1990s, examples of chip stacking often utilized just two chips to provide memory-to-microprocessor interconnection. Over time, chip stack technology evolved

to use a variety of stack configurations such as wire bonding only or chip-face-to-chip-face interconnection combined with area array solder connections, with a smaller chip (die) surface mounted to a larger die that provides interconnection to a package. Products with more complex chip stack technologies have emerged that stack two to eight or more chips and utilize perimeter wire-bond interconnections, folded flexible packaging, or a combination of flip-chip interconnection and wire-bond interconnection (see for example Web pages for Amkor, ChipPAC, IBM, Intel, Qualcomm, Samsung, Tachyon, or Tessera). Examples of hardware are shown in **Figure 4**. Figure 4(a) shows a wire-bond chip stack with a 1.4-mm plastic ball grid array (PBGA) package and less than 1.5 W power dissipation which supports approximately 100 inter-die connections and industrially available wire-bond die pitch of 100 μm with wire-bond lengths of less than 3 mm. Figure 4(b) shows a flip-chip stack and a 1.4-mm-high wire-bonded PBGA package with 2 W

power dissipation, 16-interconnect-per-mm² flip-chip connection, and 300- μ m package wire-bond-pad-to-top-die-edge interconnections. Figure 4(c) shows a thermally enhanced flip-chip stack with a 3.7-mm-high ball grid array package with lid (not shown), with 8 W power dissipation.

More recently, universities, consortia, and industry [i.e., the Fraunhofer Institute in Germany, the University of Alabama, the Association of Super-Advanced Electronic Technologies in Japan (ASET), and the Inter-university MicroElectronics Center (IMEC)] have been reporting on emerging next-generation chip stack technology and system-in-package (SIP) or system-on-package (SOP) products [14–24]. Chip stack technology research and development reports include examples of silicon through-via product opportunities and comparisons with existing wire-bond technology products. SIP and SOP reports include examples of

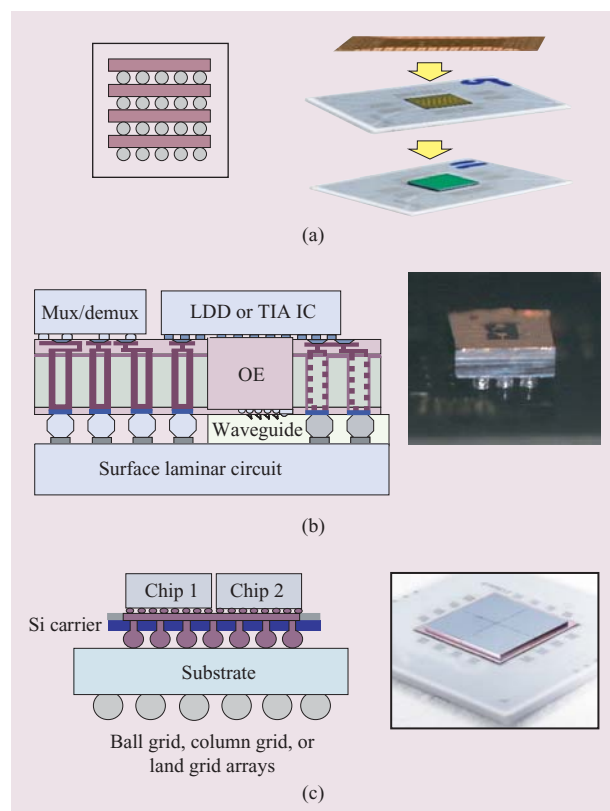


Figure 3

Examples of silicon stacks and silicon carrier applications: (a) Schematic of silicon through-via wiring chip stacking (left) and chip stack integration on package hardware (right). (b) Schematic of opto-electronic (OE) transceiver (left) and integrated transceiver hardware (right). (c) Schematic of mini-multichip module (MMCM) (left) and test vehicle hardware (right).

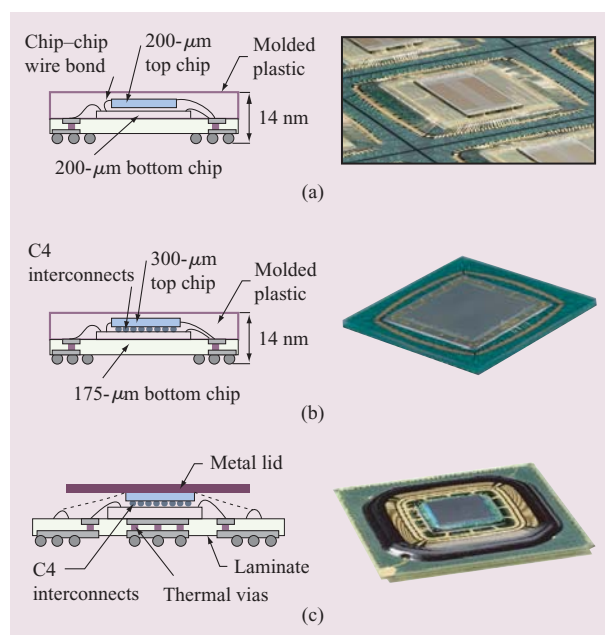


Figure 4

Schematic (left) and photograph (right) of (a) two chips which are wire-bonded using chip stacking on an organic package; (b) chip-to-chip area solder interconnection and wire bond to organic package; (c) thermally enhanced version of chip-to-chip area solder connection with wire bonding to an organic package.

traditional packaging, extension of traditional ceramic, organic, and thin-film technology with integrated passive components and two- or three-dimensional wiring integration.

Research toward a more advanced level of system integration that can be applied using chip stacking and SOP advanced package interconnection solutions has been explored from the late 1990s to the present. The SOP technology can utilize very dense I/O chip stacks, high I/O interconnection from chip to package, or integration with optoelectronic product needs. These structures can benefit from integrated passive components and integrated circuits in three-dimensional design configurations that lend themselves to miniaturization for commodity and complex products alike. The advanced integration during the 1990s and 2000s at IBM has explored leveraging semiconductor BEOL wiring ground rules that are 10 to 100 times finer than traditional packaging wiring rules and yet exploit high-yielding use of existing robust manufacturing processes and toolsets.

As at IBM, researchers in universities, consortia, and industry are exploring and reporting [14–16] on silicon through-via technology that can support high I/O density, high performance, and low cost to meet new

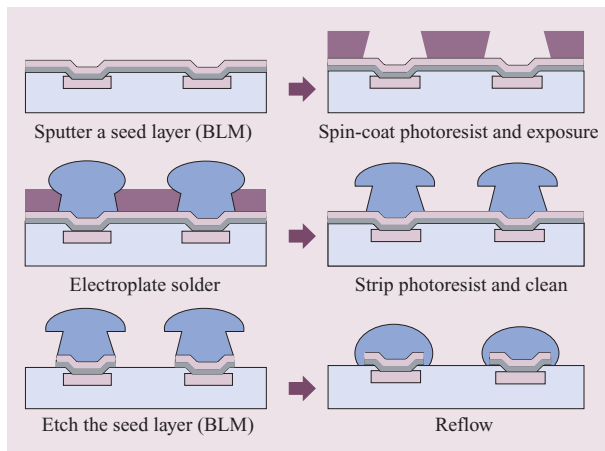


Figure 5

Microbump fabrication steps.

product application needs in ways that are not possible with today's technology design rules.

Applications and consideration for system design

The underlying benefit of system-on-package (SOP) technology is in its ability to support highly integrated modular systems or subsystems with optimized cost, size, and performance while simultaneously reducing time to market, allowing for reuse of chip design blocks (partitions) while minimizing other package- and board-level complexity.

Accordingly, one must consider not only the traditional elements of package technology, assembly, test, and reliability but also design aspects relating to the overall system functional requirements and manufacturing process. SOP technology allows multiple advanced packaging technologies to be combined to create solutions customized to each end application.

Existing market uses for SOP include RF and wireless devices—primarily cellular telephones, wireless local area networks (WLANs) and Bluetooth solutions—as well as image sensors, high-density memory flashcards, and power-supply and automotive applications. At present, SOP applications typically fall into one of three categories: modules, stacked-die packages, and stacked packages. Laminate substrates in combination with wire-bonded die stacks dominate the market, although flip-chip/wire-bond combinations are becoming increasingly available. The leading commercial applications for stacked-die chip-scale packages (CSPs) are those requiring increased memory density in a small form factor. The driving force behind the emergence of stacked CSPs has been the handset market because of the design

push for reduced dimensions combined with the proliferation of memory-hungry functions (messaging, color displays, interactive games, and other performance differentiators).

Silicon interconnection and integration

Three enabling technologies of the silicon carrier permit applications such as a single-chip module interconnection or multichip integration of heterogeneous semiconductor chips to provide a system on a package. The first is μ -C4 interconnection technology between chip and silicon carrier. The second is fine-pitch wiring and enabling silicon through-via technology, which, when combined, provide the high degree of interconnection that can support high-bandwidth integration for SOP products. The third is assembly, test, and module reliability technology that can support the desired product applications.

For multichip modules, high-I/O μ -C4 interconnection of multiple closely spaced chips allows power/ground and signals to be transferred in and out of the carrier from the module- and board-level packaging. In this scheme, each chip itself may contain a vastly greater number of I/O and power/ground connections than may be effectively handled by standard first-level packaging at present. The off-carrier connections, which drive the carrier through-via density, were intended to match the industry-standard first-level packaging C4 pitch. The carrier size may range from that of a typical large chip up to something many times greater, although through-via processing constraints demand that the carrier thickness be typically only a fraction of the usual starting thickness of a Si wafer. Below we discuss the development of the key technology elements used to build the Si carrier.

Micro-C4 interconnection development

An increase in the area array density of interconnections demands a concomitant decrease in the pitch/diameter of the solder bumps. Semiconductor test chips and silicon carrier test vehicles have been successfully fabricated with 50- μ m μ -C4 diameters on a 100- μ m pitch and 25- μ m microbump diameters on a 50- μ m pitch compared with typical industry standards of 100- μ m solder bumps on 200- μ m or 225- μ m pitches. This advance using μ -C4 interconnection represents a 16 times improvement in I/O area density over a standard flip-chip array with 200- μ m pitch. A range of solder and various ball-limiting metallurgies (BLMs)¹ were explored, including high-melt solder, PbSn (97/3), eutectic PbSn (37/63), Pb-free solder (Sn/Ag/Cu family of solders), and gold-tin [AuSn (80/20)]. Ball-limiting metallurgies studied included compositions such as TiW/CrCu/Cu/Ni/Au, Cr/CrCu/Cu/Au, Ti/Cu/Ni/Au, Ti/Ni/Au, Ti/Cu,

¹Given in wt. %.

Cr/Cu/Cu/Ni/Au, and others considered to be dependent on the solder interconnection.

A plated-through resist process was used to fabricate some of the μ -C4s, as shown in **Figure 5**. Solder-volume reduction is achieved by plating solder through a resist mask. Removal of the seed metal between the plated μ -C4 bumps is achieved using a proprietary etchant to permit negligible BLM undercut. After reflow, μ -C4 bump heights were targeted to be less than 25 μ m for both the 100- μ m-pitch and 50- μ m-pitch chips. Maximum height variation across an 8-in. wafer was less than 4 μ m.

Figure 6 shows scanning electron microscopy (SEM) views of typical reflowed μ -C4 bumps, while cross sections of joined chips of 100- μ m-pitch and 50- μ m-pitch μ -C4s are shown in **Figure 7**. For these early studies, the chip-to-carrier gaps were less than 20 μ m for the 100- μ m-pitch and 50- μ m-pitch chips, as seen respectively in **Figures 7(a)** and **7(b)**. These solder-join heights represent a dramatic reduction from the typical $\sim$ 80–100- μ m joined height for the standard 200- μ m-pitch C4 bumps used in many applications today. Electrical results for μ -C4-joined chains of 100- μ m pitches and 50- μ m pitches are plotted in **Figures 8(a)** and **8(b)**, respectively; the inset tables contain the extracted single μ -C4-join dc resistance for joins of 50- μ m and 25- μ m diameter, respectively, and for three BLM variations. Initial results suggest that improved wetting of the Ni BLM is responsible for the resultant lower overall μ -C4 join resistance seen, particularly for the finest-pitch μ -C4s.

Integration of silicon through-vias and fine-pitch wiring

Silicon-carrier-enabling silicon through-vias interconnect a chip using μ -C4 solder interconnections to provide the power and off-silicon carrier signaling wiring to the chip circuits. The use of μ -C4 solder interconnections with traditional back-end-of-chip x - y wiring can provide signal interconnection across the top surface of the Si carrier between chips. In general, the fabrication of silicon through-vias comprises the following process steps: via definition, sidewall insulation, via metallization, and connection to terminals or wiring on adjacent faces of the carrier. Each of these steps comes with its own attendant challenges related to the geometry of the via, the materials and/or processes used to insulate and metallize the vias, and the order in which these steps are performed. Myriad process flows are possible, and a variety of schemes have been proposed and developed to fabricate these connections [25–27].

In the following subsections we describe two of several technical structures and processes explored at IBM for specific application needs, each with its own advantages and disadvantages. The first illustrates one “via-first” approach considered for 300- μ m-thick silicon, the second,

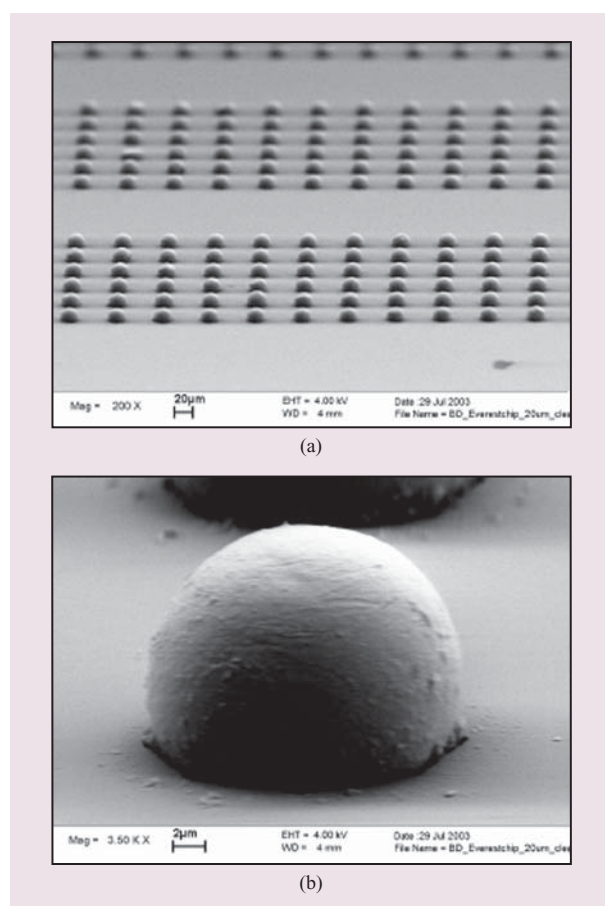


Figure 6

Examples of microbumps in which microbumps are approximately 25 μ m in diameter on a 50- μ m pitch.

a “via-last” approach that was considered for <70- μ m-thick silicon. Reviews of alternate novel structures and processes are planned for future publications.

Via first

The via-first scheme describes a sequence in which the silicon through-vias are etched, insulated, and metallized before the BEOL wiring levels are built on the carrier. In the via-last scheme, the BEOL wiring levels are built first, and the through-via steps are completed subsequent to BEOL wiring and wafer thinning. **Table 1** shows an example of process flow comparison between the via-first and via-last approaches.

One advantage of the via-first approach is the ability to fabricate freestanding Si carriers in the thickness range of 200–300+ μ m. In this technical structure, deep through-vias with high aspect ratios for wafer-level processing were sought. Electrical interconnects extending through

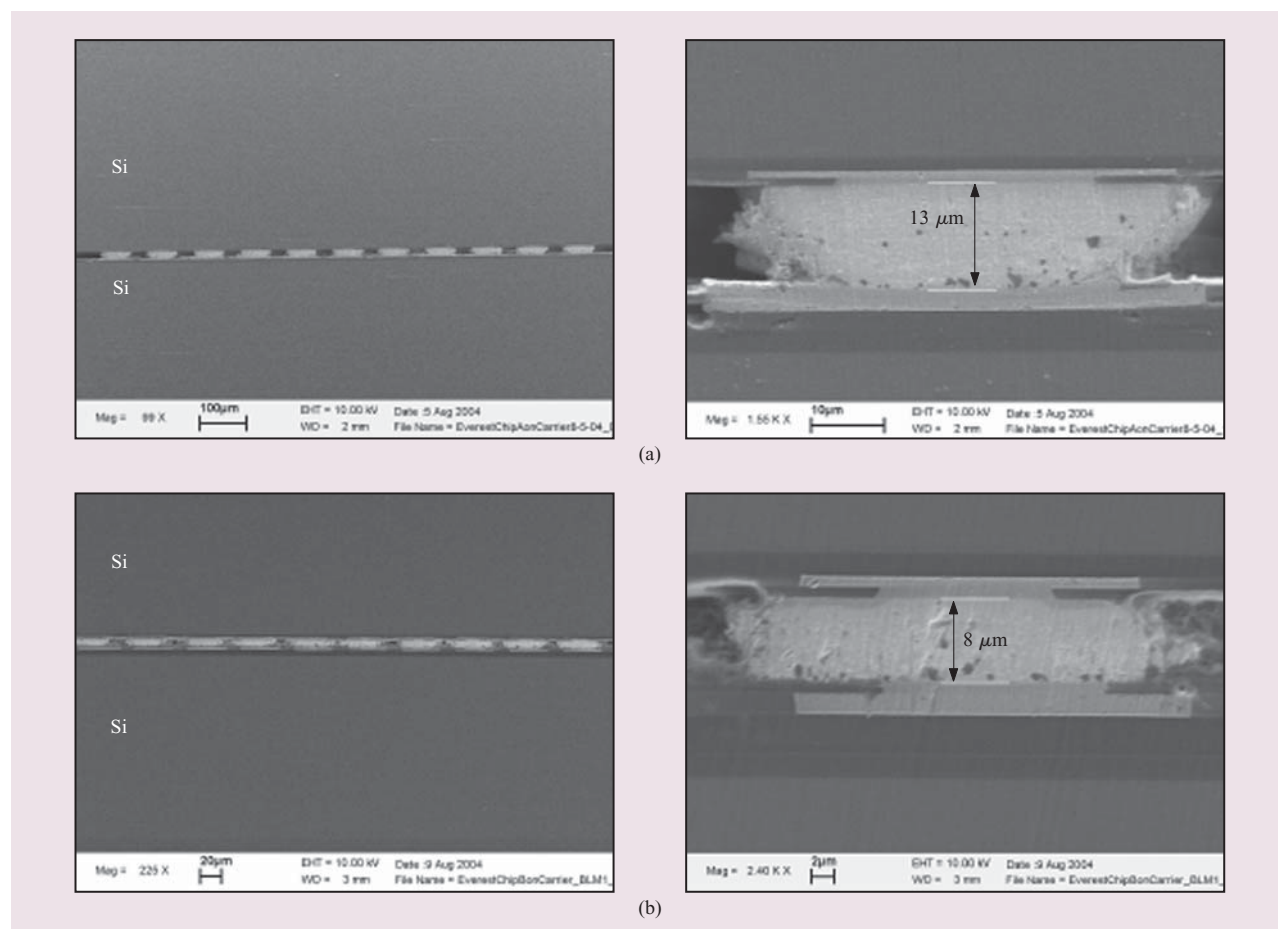


Figure 7

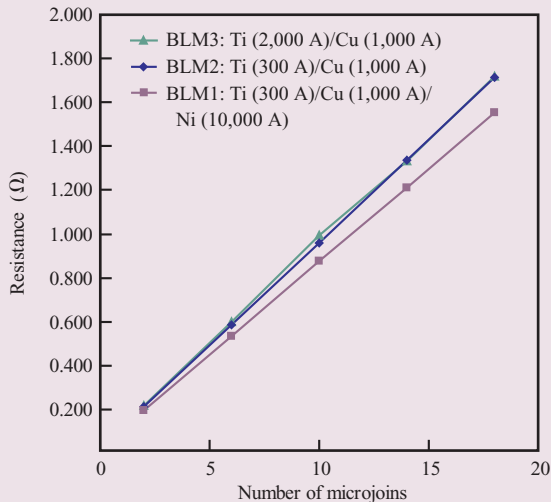
(a) Cross sections of silicon on silicon with solder connections at 100-μm pitch (left) and one 50-μm-wide solder interconnection (right). (b) Cross sections of silicon on silicon at 50-μm pitch with multiple solder connections (left) and one 25-μm-wide solder connection (right).

Table 1 Comparison of process sequence for via-first and via-last process steps to form silicon through-vias.

Process sequence	Via first	Via last
1	Form vias in wafer (i.e., RIE)	Fabricate wiring on wafer (i.e., BEOL)
2	Form or deposit dielectric	Mount wafer on mechanical carrier and thin wafer
3	Form liner on sidewall and fill via with conductor	Align and form vias from back of wafer to contact metallization/wiring from step 1 above
4	Fabricate wiring on wafer (i.e., BEOL)	Form or deposit dielectric
5	Thin back side of wafer to contact Si through-vias	Form liner on sidewall and fill via with conductor
6	Form interconnections on back of wafer	Form interconnections on back of wafer

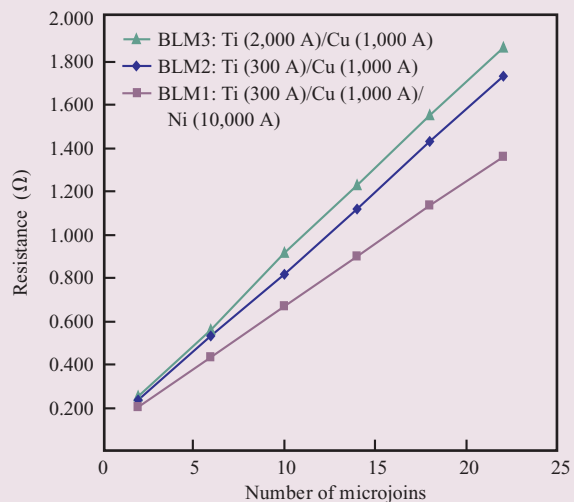
the carrier were fabricated by first defining vias in the silicon. The deep via definition could be achieved through several methods, including Bosch-type reactive ion etch (RIE), cryogenic RIE etch, and various forms of

isotropic/anisotropic wet etch [28]. In this fabrication, Bosch-type deep RIE was used because the alternating deposition and passivation steps of Bosch etching allowed for the formation of through-vias with smooth, straight



	BLM1	BLM2	BLM3
R (mΩ)	27	28	30

(a)



	BLM1	BLM2	BLM3
R (mΩ)	32	39	41

(b)

Figure 8

Resistance R through multiple solder interconnections for (a) 100- μm pitch and (b) 50- μm pitch. Each pitch illustrates a few representative ball-limiting metallurgies that were characterized for eutectic solder.

sidewalls to a depth of 300 μm . After the vias were defined, various insulating films were added to provide electrical insulation between the silicon and the metal within vias. Films were prepared by techniques that included thermal, plasma-enhanced chemical vapor deposition (PECVD) using silane, and tetraethoxysilane (TEOS)-type oxides, as well as low-pressure chemical vapor deposition (LPCVD) nitrides. Following insulation, the vias were ready for metallization.

The deep via may be filled by copper plating [29] or paste filling [30–33]. The ASET Laboratory in Japan has demonstrated a mechanical stack of four chips connected by silicon through-vias of 10- μm diameter and 50- μm depth, fully plated with Cu and joined with solder contacts between the layers [34–36]. Fully plated, narrow, relatively shallow silicon through-vias have been demonstrated to work. However, when the carrier thickness is increased, the coefficient of thermal expansion (CTE) mismatch between silicon (3 ppm/°C) and copper (16 ppm/°C) becomes significant. Thermo-mechanical modeling of a 50- μm -diameter, 200- μm -deep, fully plated Cu via shows that the Cu can expand upward by 0.35 μm at the center of the via upon repeated thermal cycling during subsequent CMOS processing. If the via structure is not properly designed, copper expansion can result in interlayer dielectric (ILD) and silicon cracking. Thus, the choice of specific via diameter and silicon

wafer thickness becomes important; one solution to accommodate thick silicon through-vias is to fill some significant portion of the deep vias with material having a CTE comparable to that of silicon.

Tungsten (W) and molybdenum (Mo) are metals with low CTE (4.5 ppm/°C and 4.8 ppm/°C, respectively). Physical vapor deposition (PVD), or sputter, techniques may be used for small via sizes, but the process is too slow and may not meet the conformality requirements for the Si carrier applications with deep vias. Chemical-vapor-deposited (CVD) tungsten is an interesting front-end-of-line (FEOL) conformal metallization choice, but it is practically limited to a deposition of a few micrometers using standard techniques, and typical as-deposited films are highly stressed. Laser-assisted CVD of W or Mo is significantly faster, and the process could be used for filling the deep vias with these or other low-CTE metals and/or ceramics [37–40]. These structures and processes are not included in the present assessment summary. Fill materials derived from different metal–ceramic composites exhibit adequately low ($\ll 16$ ppm/°C) CTEs. One such material is a copper–ceramic three-dimensional composite that is used in the fabrication of multilayer ceramic (MLC) chip carrier conductive vias. This type of 3D composite alone or in combination with plated Cu deep via walls may be used for conductive through-via filling. Plated Cu thickness on the deep via walls may be

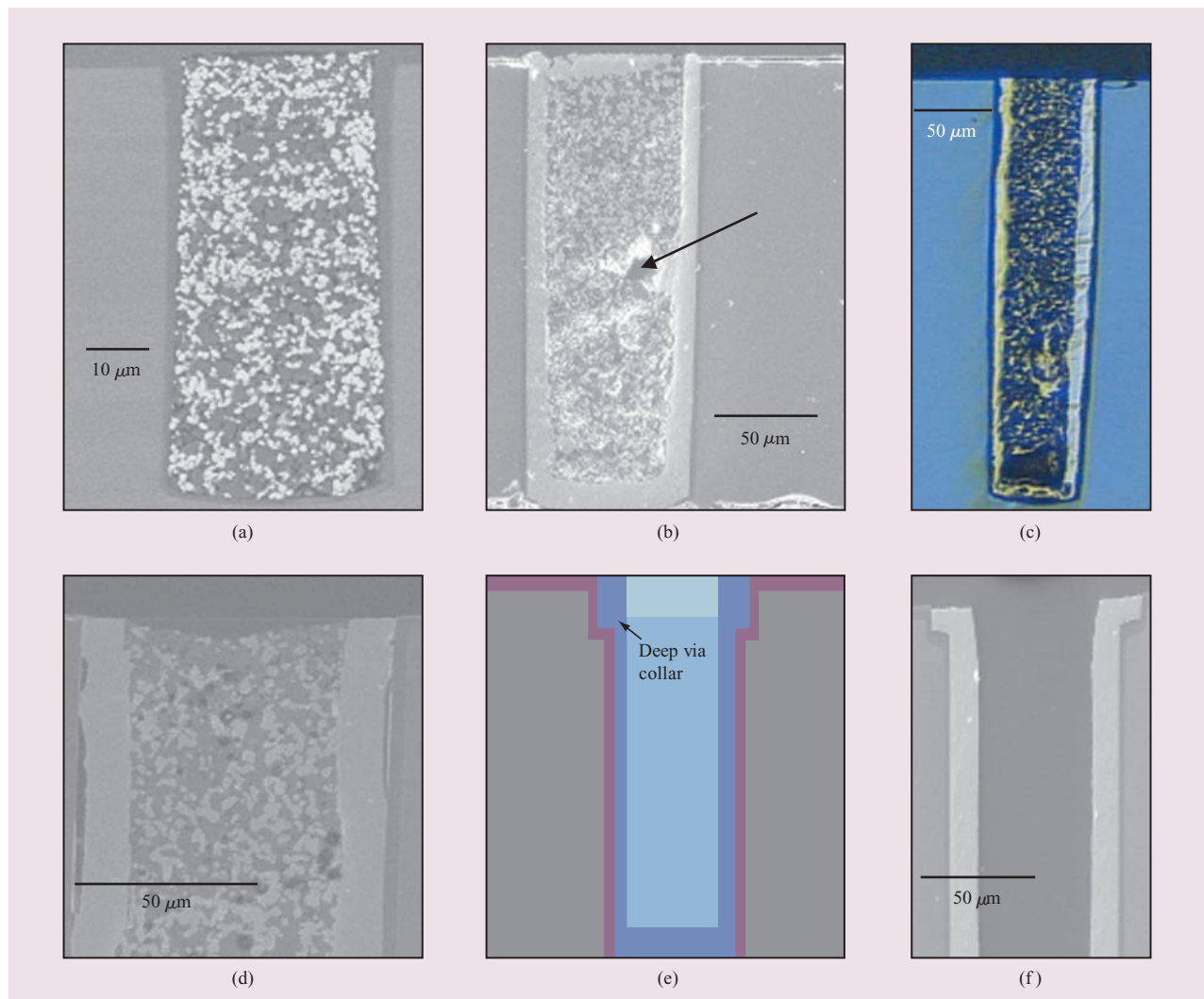


Figure 9

(a) Small composite-filled via; (b) larger via with copper partial plate, with composite fill showing small inclusion void; (c) optical via image with partial plating and composite void; (d) secondary electron microscope image of via with partial plated copper and composite fill; (e) schematic of via cross section with via collar used to contact back-end-of-line wiring and vias along with composite via fill; (f) scanning electron microscope photograph of copper-lined via with collar.

limited to a few micrometers, which can provide excellent conductivity at high frequencies.

The difficulty of filling a deep, blind via increases significantly with the via depth. It is relatively straightforward to fill vias of 1:1 aspect ratio, but vias approaching 300- μm depth and aspect ratios of 4:1 to more than 10:1 require specialized processes. **Figure 9** shows examples of vias. Figure 9(a) shows a via filled with copper-ceramic composite in one application; Figure 9(b) shows a via with combined plated copper and copper-ceramic composite, where an internal void proved to be inconsequential. Figure 9(c) shows an example of

incomplete composite fill at the bottom of the via with a non-optimized fill process, and Figure 9(d) a secondary backscatter via image. The deepest-aspect-ratio vias required more than one composite fill application. The schematic of the via in Figure 9(e) shows a collar design for deep through-vias along with conductor, composite, and seal. Figure 9(f) shows a sample cross section of the conductor with collar prior to the composite fill process. These through-silicon composite-structure vias for silicon of approximately 300- μm thickness were shown to support BEOL processing, thermal cycling, and electrical and mechanical stressing.

The size of a void retained in a composite via is a function of the chamber vacuum during the fill process [41]. Minimum void diameter approximated from the level of vacuum is about 5 μm . However, dynamic evacuation of the chamber results in another issue in paste filling of vias: solvent evaporation. At present, it is not clear how significant a role the solvent evaporation plays in void formation in the deep blind vias. However, paste drying is noticed during the very-low-vacuum fill process.

Okuno et al. [30–32, 41] and Matsuda et al. [42] suggest the use of paste without an evaporable component. Epoxy-based chip underfill materials are an example of this type of approach [43]. However, epoxies are not adequately thermally stable to allow exposure to standard CMOS BEOL processing temperatures, which limits their utility in the silicon carrier application.

After the vias are filled, the low-temperature stable carrier is removed, and the composite via is taken through process steps to create a cohesively strong, sealed structure ready for additional processing. Next, the BEOL processing of wiring levels above the deep-via wafers is performed with dielectric deposition using PECVD.

A key element in building single- or dual-damascene Cu wiring above deep silicon through-vias is making the electrical connection between the wiring and the through-via. As discussed above, the deep through-silicon via structure permits standard BEOL processing. The BEOL connection to the silicon through-via was made using a collar around the deep via; this collar, plated with Cu, provides a solid contact plane, as shown in the schematic cross section of **Figure 10**.

The silicon-based substrate approach leverages current- and previous-silicon-generation tools to achieve very dense wiring, meeting future I/O pitch and wiring requirements. Standard BEOL processes and wiring ground rules will enable high-yield and low-cost fabrication of these carriers. The same toolsets and processes can be extended to fabricate thicker “fat wires” as needed. Silicon carrier test structures include wiring dimensions ranging from 1- μm to 10- μm lines and spaces, with Cu thicknesses ranging from 1 μm to 4 μm . While wider, longer, and thicker than standard CMOS “fat-wire” levels on most chip designs, these BEOL wiring levels were fabricated using existing single- and dual-damascene Cu processes. An example of a three-level build with silicon through-vias is shown in **Figure 11**, where two patterned Cu planes (power and ground) extend underneath an impedance-matched differential signal level, and where each signal line is connected to the collar of a through-via.

Via last

Another approach to integrating wiring and through-vias is to build the wiring first and create the through-vias

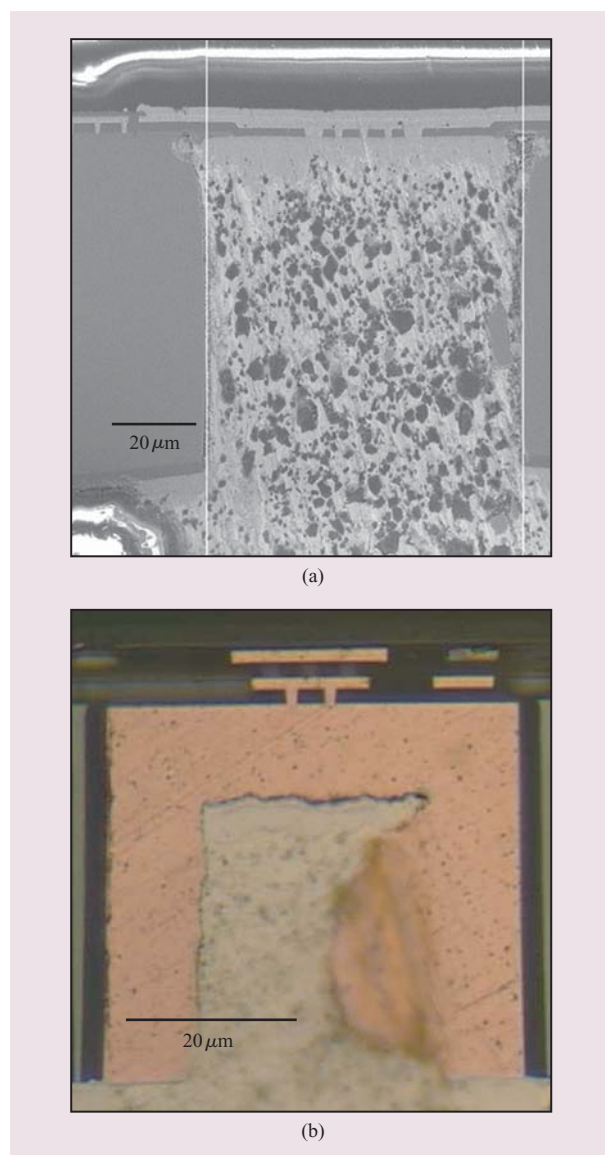


Figure 10

(a) Silicon cross section with trench-decoupling capacitors and back-end-of-line thin deposit copper via interconnection to solder “via last” process for silicon through-via where polished cross section left abrasive embedded (dark spots) in the solder. (b) Test vehicle with copper wiring, vias, and thick-walled copper deposition and solder interconnection as “via last.” Note portion of Cu pushed into solder on right of silicon through-via during sample polishing.

later. In this second approach, dubbed “via-last,” the process begins with a fully processed wafer containing all of the BEOL wiring levels and top-side micro-joined terminal pads finished with a solder-wettable barrier coating such as Ni/Au. This method is particularly useful for the fabrication of silicon carriers with thicknesses less

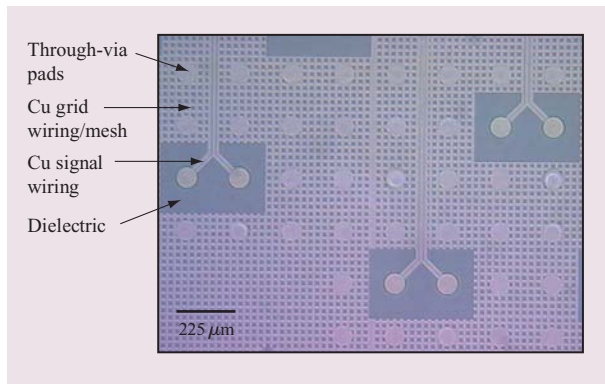


Figure 11

Example of a three-level structure with silicon through-vias and two copper planes.

than $\sim 200\ \mu\text{m}$; however, processing of very thin wafers requires a handler wafer to be attached to the front side. Moreover, this handler/wafer combination must stand up to typical BEOL vacuum processing steps such as PECVD insulator deposition at $\sim 350^\circ\text{C}$, but ultimately the handler must be easily removable (in this case, once the diced carriers have been bonded to the first-level package). Reversible wafer bonding has been used for wafer-thinning applications for some time now [44]. Dragoi et al. [45] discuss the application of reversible bonding of wafers using low-temperature-melting waxes or adhesive tapes which lose adhesion at elevated temperature or under ultraviolet light (UV) exposure, or are dissolved using solvent exposure [46]. An alternative to the above handler wafer release options is to etch the handler wafer completely to an etch-stop layer previously deposited on its surface [45].

In the Landesberger et al. application [44], not only is the wafer thinned down to $20\text{-}\mu\text{m}$ thickness, but as the wafer is thinned, the individual chips are simultaneously formed (singulated). Singulation is based on etching sufficiently deep trenches around the chip, which is then exposed during the thinning process, thus separating the chips from one another. One benefit of this approach is that the corners can be rounded, thus reducing the possibility of cracking of the thinned chips. The narrower “dicing channel” reduces the loss of silicon surface area.

The low-temperature-stable materials (maximum temperature $< 200^\circ\text{C}$) used by Landesberger et al. and Dragoi et al. [44, 45] are not practical for the silicon carrier application, where high-temperature CMOS processing is necessary while the thinned silicon wafer is still bound to the handler wafer. Thus, a high-temperature-stable laminated stack is required.

Stoffel et al. [47] describe in principle the method by which wafer lamination using high-temperature

polyimides can be achieved. The basic principle for handler wafer lamination to the product wafer is the use of high-temperature thermoplastic polyimide adhesive, such as oxydiphenylene oxydiphthalimide (ODPA-ODA) polyimide. The critical property with the thermoplastic polyimide is that its glass transition temperature (T_g) is relatively low, so that appreciable flow can occur during lamination to bring the device and the handler wafers to intimate contact without leaving voids at the bond line. ODPA-ODA ($T_g = 270^\circ\text{C}$) will experience flow during the lamination process under pressure and lamination temperature $\gg T_g$ of the thermoplastic adhesive, thus creating a good bond between the device and the handler wafers. Thermal, UV light, solvent, or other such approaches will not be able to attack polyimides in any reasonable fashion at wafer level. However, laser ablation of polyimides is well known [48–51]. Thus, with clever planning using an appropriate laser-transparent handler wafer, the polyimide can be ablated and the handler thus released from the structure.

In the silicon carrier via-last process exercised here, the wafer with completed BEOL wiring including Au pads is bonded to the glass handler wafer using pyromellitic dianhydride oxydianiline (PMDA-ODA) polyimide and a thermoplastic polyimide with low T_g as the adhesive; these are coated and cured on the device wafer. Optical characteristics of the handler glass, which must be considered for laser release processing, are a function of the glass thickness. The selected thickness is comparable to an 8-in. wafer thickness. Using a 308-nm laser light wavelength, which was the wavelength of choice for our initial handler wafer release process [49], this glass transmits about 80% of the laser energy.

Once laminated, the wafer is thinned to the desired target depth using standard back-side grind and polish techniques, after which photolithographic patterning is performed on the wafer back side. For the glass handler used in this work, a back-side alignment tool was used to align the through-via level to the carrier front-side pads. Once the back side of the silicon wafer is patterned, deep anisotropic etching is carried out, in this case using a deep RIE tool. Although the Bosch process [52] is highly selective to oxide, the silicon etch is quite aggressive ($\sim 6\ \mu\text{m}/\text{min}$) and requires a decrease in the etching rate at the via bottom. Care must be taken not to over-etch once the BEOL contact level has been reached at the base of vias; otherwise, the passivation of the via sidewall close to the foot of the via can be compromised by the formation of a silicon undercut. This is especially undesirable because the via-last process precludes the possibility of using high-temperature, highly conformal insulation processes such as thermal oxidation or LPCVD deposition. In our study, PECVD deposition was utilized, with a controlled sidewall insulation thickness from the

top of the via to the base. Sidewall insulator thickness was managed with top to bottom thickness about $2\times$ to $3\times$ depending on the PECVD tooling and process temperature. Before metallization can occur, the insulator at the base of the through-via must be removed without damaging the sidewall. Control with knowledge of the difference in oxide thickness at the base of the via and at the surface of the wafer allowed the use of maskless RIE as a means of opening the base while keeping sufficient insulation on the back side of the wafer and the sidewalls. Once again, care must be taken not to over-etch in order to avoid degradation of the thinnest sidewall insulator near the via base.

Following opening of the insulation, standard PVD liner/seed, plating, and CMP are used to partially plate a skin of Cu of $\sim 2\ \mu\text{m}$ to $\sim 5\ \mu\text{m}$ on the walls of the through-via. A cleaning process is used to ensure that all CMP residue is removed from the via before the wafer is sent for terminal metal deposition. In this work, standard Cr/Cu BLM and high-melting-temperature Pb/Sn solder were evaporated using a molybdenum shadow mask. Following evaporation, the wafers were sent through a hydrogen reflow oven. The solder was allowed to flow directly into the Cu-lined via, although future plans include filling of the central void with a stable, CTE-matched filler before BLM/solder deposition to avoid long-term reliability issues due to CTE mismatch among solder, Cu, and Si. A cross section of a via-last metallized via is shown in Figure 10. The dark debris seen in the via is due to the entrapment of polishing slurry during SEM section preparation. Note the contact vias making the connection from the center of the via to the metal line above it.

Integration of passive and/or active circuit technology

The active surface of the silicon carrier can be used for high-density top-die interconnect wiring and can also serve to support local integrated passive elements and/or active circuit technology depending on the application design.

To demonstrate this concept, a passive-technology test vehicle assessment was made. Here, a conventional flip-chip-on-ceramic-module structure was assembled with the insertion of a silicon carrier with integrated decoupling capacitance (decap) between the die and the substrate. The silicon carrier with integrated decoupling capacitance was measured to have more than $2.5\ \mu\text{F}/\text{cm}^2$ decoupling capacitance. Chip ground and voltage connections were made from silicon carrier to chip and tied to trench-based capacitor array terminals used in this test vehicle demonstration (Figure 12 and, as shown in schematic cross section, Figure 13). Hardware modeling and characterization results indicated that an opportunity

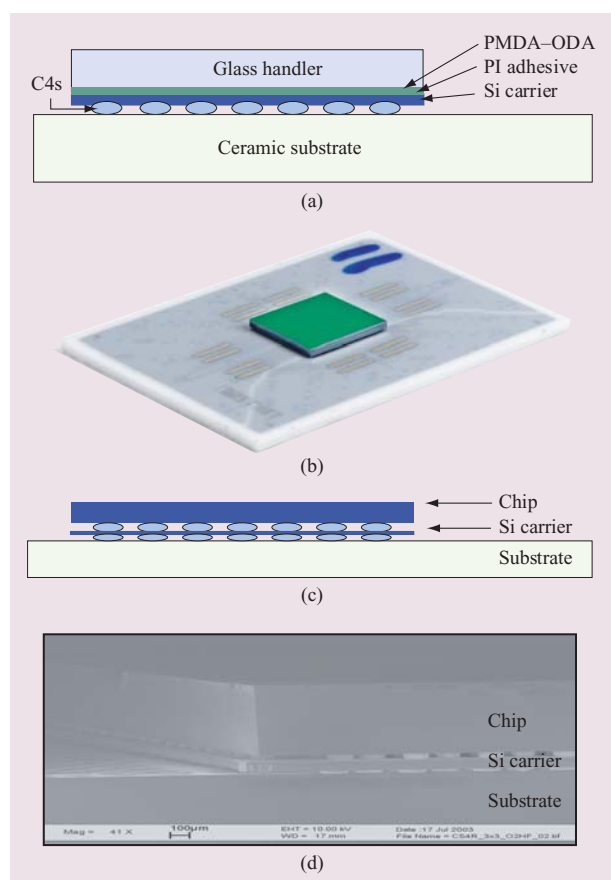


Figure 12

(a) Schematic of Si carrier bonded to ceramic substrate prior to glass handler release; (b) chip, silicon interposer, and substrate; (c) schematic of silicon interposer stack; (d) an actual stack.

exists to suppress noise for high- or mid-range-frequency applications.

Chip- and package-level integration

Once silicon wafers have been processed as 1) self-supporting, with wafer thicknesses of 200 to 300+ μm or 2) mechanically supported forms with wafer thickness of less than 100 μm , the wafers go through dicing, cleaning, and bonding processes as well as removal of the mechanical support structure for stacked or Si-carrier-thinned structures. Depending on the structure to be fabricated, $\mu\text{-C4s}$ may also be added prior to dicing through subsequent processing at the wafer level to join to an adjacent structure.

The self-supporting wafers can be diced using standard wafer-dicing operations. These structures can then be handled similarly to chips and undergo chemical cleaning and bonding.

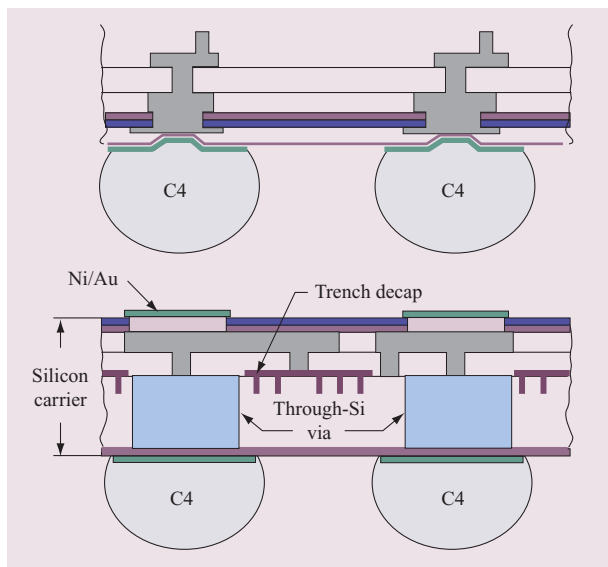


Figure 13

Schematic diagram of chip and silicon carrier package interconnection with solder C4 interconnections and example of use with trench capacitors for decoupling. (C4 = controlled collapse chip connection.)

The mechanically supported structures are etched or diced through the wafer and either partially or fully through the mechanical supporting structure. Taking the latter case as an example, silicon carrier structures have been fabricated and joined to a supporting organic or ceramic carrier, and the mechanical support has been removed using a combination of process steps including laser release and chemical and thermal cleaning. For chip stack structures, mechanically held wafers can be wafer-joined to adjacent wafers or thinned wafer die-stack structures followed by removal of the mechanical support structure and subsequent cleaning. A thermal or laser release process may be utilized to release the mechanical support structure. Details below describe the IBM laser release process.

The selection of pulsed UV laser over visible or IR laser for the release process is due primarily to the ability of the former to control the etch depth by the number of pulses and the fluence, and the lack of obvious thermal damage to the substrate. A typical UV laser pulse width is about 20–30 ns, with laser energy of about 450 mJ. Beam size at the sample surface may be approximately 0.5–1.5 cm², resulting in fluences ranging from 900 mJ/cm² to 300 mJ/cm² if no losses are experienced due to laser optics.

The PMDA-ODA polyimide (PI) laser ablation threshold (308 nm) is about 50 mJ/cm² [48]. It should be noted that even with fluences below the ablation

threshold, large stress pulses are generated in the structure. It has been reported that a stress pulse of $\sim 10^4$ Pa is experienced in PMDA-ODA PI film when it is exposed to ~ 10 -mJ/cm² fluence, which is significantly below the threshold for ablation [50, 51]. However, Doany and Narayan [48] report that using fluences up to 100 mJ/cm² did not cause damage to a metal-polymer thin-film wiring structure, even when the PI thickness was only 3 μ m.

One example of the handler wafer release in the silicon carrier application occurs at the singulated, C4-bonded state, shown as a schematic cross section in Figure 12(a). Demonstrations of singulated Si carrier join to substrate and chip-to-silicon carrier join have been developed. Silicon-carrier-to-substrate pitch assemblies were at 200 μ m, and chip-to-silicon-carrier joining was developed at both 100- μ m and 50- μ m pitches. As described above, subsequent to the attachment of the silicon carrier to the substrate, release and cleaning of the carrier surface (which had been attached to the handler) are completed to remove any polymer residue. The I/O pads are cleaned, and the fine-pitch I/O chip is bonded to the Si carrier surface as shown in Figures 12(b), 12(c), and 12(d).

Electrical performance characterization

The two main building blocks for signal interconnects on Si carriers are the (horizontal) wiring and the (vertical) through-vias. The electrical performance of these components is typically characterized both in time and frequency domains, with low- to mid-range data-rate applications placing the emphasis on the time domain and high-end data-rate applications more on the frequency domain. The following typical characterization examples show the electrical performance potential of these Si carrier components.

Coplanar waveguides for applications with low- to mid-range data rates (≤ 10 Gb/s)

Using silicon carrier technology, for example for an electro-optic transceiver (EOT) or a mini-multichip module (MMCM), the first example (Figure 14), as (a) cross section and (b) and (c) top views for ground-signal-ground (GSG) and ground-signal-signal-ground (GSSG), respectively, consists of co-planar waveguides (CPWs) which were characterized in a time domain using a short-pulse propagation technique. The input source pulse had a 197.5-mV amplitude and a 39.8-ps rise time. In the first example, the output pulse at the end of the line was recorded and compared to the input. The copper conductor thickness was varied as 2, 3, and 4 μ m and line length as 0.25, 1, and 5 mm.

Table 2 shows the extracted delay measured at the 50% level of the propagated signal, propagated rise time, t_r , between the 10% and 90% levels, signal amplitude,

Table 2 Time domain measurement results of co-planar waveguide (CPW) transmission.

	Length (mm)	Delay (ps)	t_r (ps)	V (mV)	f_{-3dB} (GHz)	τ (ps/cm)
$t = 2 \mu\text{m}$	0.2	4.8	42.4	193.8	8.9	
	1	12.2	43	191.3	8.8	
	5	37.2	63.6	175	6	62.5
$t = 3 \mu\text{m}$	0.2	4	41.8	195	9.1	
	1	10.6	44.8	191.3	8.5	
	5	34	61.6	182.5	6.2	58.5
$t = 4 \mu\text{m}$	0.2	4.6	43	196.3	8.8	
	1	10.6	46.2	193.8	8.2	
	5	37.2	64	186.3	5.9	66.5

–3-dB frequency points, and propagation delay per unit length, τ .

The interconnect bandwidth is defined as follows. One can consider the interconnect to act as a low-pass filter that has a “upper-3 dB” frequency of $f_C = 1/2\pi RC$. For such an “RC” representation, $t_r = 2.2 RC = 0.35f_C$. In order to maintain distortionless propagation, the critical frequency f_C should be equal to the inverse of the pulse width, p_W , which is also the data-bit or cycle time. This means that $t_r < 0.35 p_W$. As can be seen, a bandwidth of approximately 8.5 GHz can be achieved for 1-mm-long lines, and a bandwidth of approximately 6.0 GHz for 5-mm-long lines. This is adequate to support several-gigabit-per-second (Gb/s) data rates over short line lengths.

A slight improvement in bandwidth is observed when the conductor thickness is varied from $2 \mu\text{m}$ to $3 \mu\text{m}$. Although the $2\text{-}\mu\text{m}$ -thick lines had a resistance of $22.3 \Omega/\text{cm}$, which is 2.3 times higher than for the $4\text{-}\mu\text{m}$ lines, the bandwidth for the thicker, 5-mm-long lines was actually lower—5.9 GHz vs. 6 GHz. This is because the measured capacitance was actually higher by 41% for the $4\text{-}\mu\text{m}$ -thick lines—1.4 pF/cm vs. 0.97 pF/cm. The $3\text{-}\mu\text{m}$ -thick lines had a slightly better bandwidth of 6.2 GHz. The line capacitance values were respectively 0.97, 1.05, and 1.37 pF/cm, and the line resistances were 22.3, 13.8, and $9.65 \Omega/\text{cm}$, for 2-, 3-, and $4\text{-}\mu\text{m}$ metal thickness and $5\text{-}\mu\text{m}$ width. These lines are a first attempt at fabricating a complex silicon carrier structure. Future test sites will have optimized cross sections (width to space to dielectric height) for better high-speed performance. The degradation when going to $4\text{-}\mu\text{m}$ -thick lines is due to the increase in line capacitance per unit length, which is greater than the decrease in resistance per unit length, thus increasing the propagation delay and rise time.

The $5\text{-}\mu\text{m}$ -wide lines were also cross-sectioned. The line widths were $4.9 \mu\text{m}$, the spacings were $5.1 \mu\text{m}$, the thickness was $1.8 \mu\text{m}$, and the height above the silicon was $2.0 \mu\text{m}$. A thin nitride layer above the lines had $0.63\text{-}\mu\text{m}$ thickness, with a dielectric constant of 7. On the

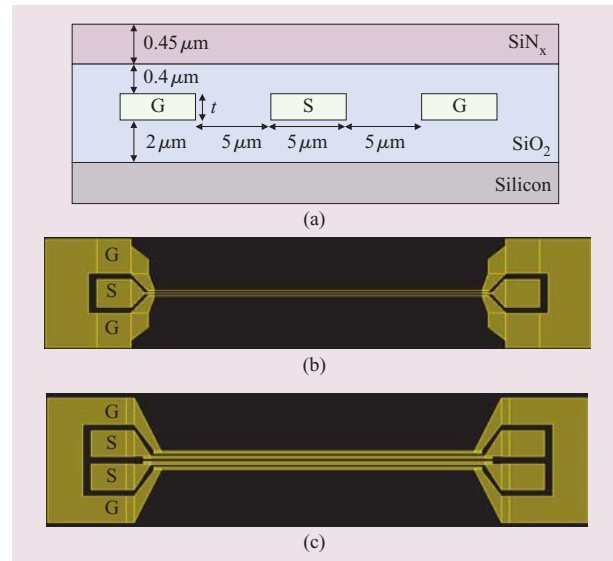


Figure 14

Coplanar waveguide (CPW) showing (a) cross section where t was varied as 2, 3, and $4 \mu\text{m}$; (b) ground-signal-ground (GSG) test structure; (c) test structure to measure coupling effects between signal lines with ground-signal-signal-ground (GSSG) launching pads for time domain measurements. The metal is copper and the silicon is low-resistivity ($10 \Omega\text{-cm}$ range).

basis of these dimensions and the measured resistance per unit length of $22.4 \Omega/\text{cm}$, the metal resistivity was found to be $1.95 \mu\Omega\text{-cm}$. The calculated capacitance was $C_{\text{calc}} = 0.96 \text{ pF/cm}$, while the measured value was $C_{\text{meas}} = 0.97 \text{ pF/cm}$, or a difference of only 0.4%. These material parameters were then used to obtain a transmission-line model with frequency-dependent $R(f)L(f)CG$ parameters per unit length using the IBM-developed CZ2D, a method-of-moment electromagnetic field solver. The IBM PowerSpice circuit simulator was used to simulate signal propagation along the 5-mm-long line. The source had the same 197.5-mV amplitude and a 39.8-ps rise time, as indicated above for the TDT measurement. Both the source impedance and the termination were 50Ω . **Table 3** shows the excellent correlation between measured and simulated results.

Coupling effects were also studied between the lines of similar dimensions with line length fixed at 1 mm with the ground-signal-signal-ground structure shown later in Figure 17. The width, thickness, and spacing of the conductors are listed in **Table 4** along with measured far-end noise. In this case, only the step source and detected line ends are $50\text{-}\Omega$ -terminated, while the active-line end and the near-end quiet-line end are open-ended. Crosstalk would be half the amplitude listed in Table 3 if all ends were terminated.

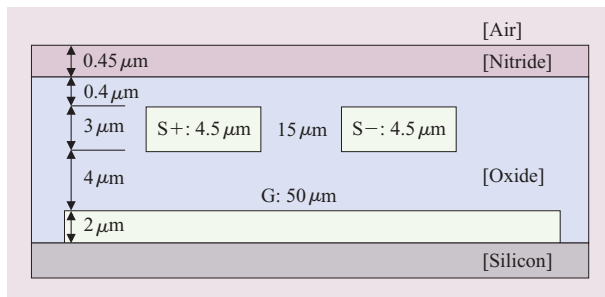


Figure 15

Differential pair cross section showing signal lines and reference plane.

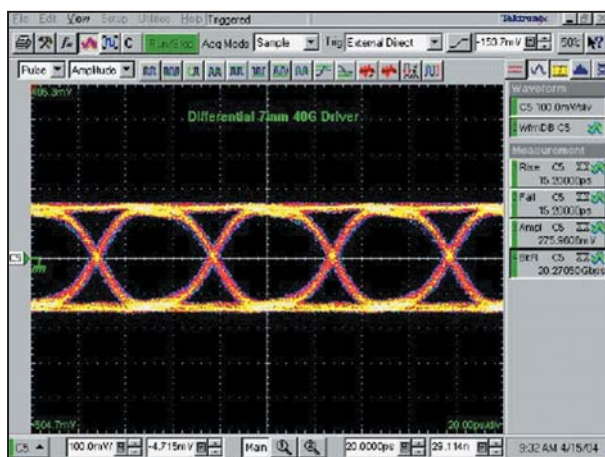


Figure 16

Eye diagram (20 Gb/s) for 7-mm differential microstrip lines with pseudo-random bit sequence (PRBS) 7-1 data pattern.

Measured far-end noise is less than 14% and can be as low as 11.5%. Compared with the -3-dB frequency, a similar trend is observed, in which lines having a thickness of 3 μm have better performance compared with those of 2- μm thickness. The performance begins to degrade when line thickness is further increased to 4 μm . Overall, crosstalk is similar to values encountered on package interconnects and much lower than for on-chip wiring. The silicon carrier can thus extend the bandwidth of on-chip wiring owing to the lower loss, and can also offer high wiring density owing to the lower noise levels shown.

Differential microstrips for applications with high data rates (≥ 10 Gb/s)

The next example involves differential microstrip lines for high-data-rate applications (10 Gb/s and beyond), as

Table 3 Correlation between measured and simulated signal propagation on 5-mm-long line with 5-mm width and space.

	Measured	Simulated	D (%)
Voltage (mV)	175.0	177.0	+1.1
Delay (ps)	37.2	35.6	-4.3
Rise time (ps)	63.0	59.7	-5.2
C (pF/cm)	0.96875	0.96495	-0.4
L (nH/cm)		3.9917	
Z_0 (W)		64.3	
t (ps/cm)	74.4	1.2	-4.3

Table 4 Measured far-end noise for coupled-line structures (input source pulse had 197.5-mV amplitude and 39.8-ps rise time).

	Length (mm)	Width of S1 and S2 (μm)	Space (μm)	Ground width (μm)	Far-end noise (%)
$t = 2 \mu\text{m}$	1	5	5	5	13.50
	1	5	10	5	11.70
	1	10	10	10	13.40
	1	10	15	10	12.70
$t = 3 \mu\text{m}$	1	5	5	5	13.40
	1	5	10	5	11.50
	1	10	10	10	13.00
	1	10	15	10	11.90
$t = 4 \mu\text{m}$	1	5	5	5	14.30
	1	5	10	5	12.60
	1	10	10	10	13.90
	1	10	15	10	12.90

shown in **Figure 15**. In contrast to the co-planar waveguide (CPW) structures, the signal conductors were shielded against the lossy silicon substrate, thus reducing the overall attenuation. The lines are designed to meet $100 \pm 10 \Omega$ differential impedance, while the CPWs were single-ended and not impedance-controlled. As will be seen, this results in a substantial gain in bandwidth.

Test structures showed line lengths ranging from 0.5 mm to 17 mm. The microstrips were contacted using ground-signal-signal-ground (GSSG) microprobes. Eye diagram measurements showed that the lines were capable of transmitting 20-Gb/s data over several millimeters. For example, **Figure 16** shows an acceptable eye opening for a 7-mm microstrip length at 20 Gb/s.

Frequency domain measurements were performed using a vector network analyzer that was calibrated up to the probe tips using a reference calibration substrate and the short-open-load-through (SOLT) technique. The attenuation was extracted from the S-parameters (**Figure 17**) using the eigenvalue analysis of the cascaded T-parameters of microstrip lines of different lengths [53, 54]. It can be concluded that the total attenuation

at 20 GHz for 7 mm is about 3 dB; i.e., the bandwidth is 20 GHz for this line length. This is far beyond the 6-GHz bandwidth that could be achieved for only 5-mm-long CPWs. As can be seen, the match to simulation is very good considering the fact that the resistivity of the metal can vary in the range indicated.

By doing simulated parameter studies, it was found that the attenuation is completely dominated by the conductor losses. Losses in the oxide are negligible. Also, the presence of the silicon does not play a role—it is sufficiently shielded by the ground plane.

From the simulations, the (differential) characteristic impedance could be determined to be around 105 Ω at 40 GHz. This is good enough for a 100- Ω design point with the usual $\pm 10\%$ margin. However, it shows that the lines are slightly too narrow, and that a wider line (e.g., 5 μm instead of 4.5 μm) might be more appropriate. An increase in line width simultaneously decreases the impedance and the attenuation.

Overall, it can be stated that high-data-rate transmission (10 Gb/s and beyond) can easily be achieved over several mm using this differential microstrip structure.

Through-via inductance

The final example (Figure 18) consists of three vias with a center via (S) as the signal line strapped at the bottom to two return vias (G). The total via diameter was 70 μm and the via pitch was 100 μm . Two wafers with thicknesses of 185 μm and 271 μm were measured at ground-signal-ground (GSG) sites. The sites were strapped on the back with either 500- μm by 625- μm or 200- μm by 625- μm straps. The structures were probed with a GSG microprobe, and the reflection coefficient was measured with a vector network analyzer from 45 MHz to 40 GHz after short–open–load (SOL) calibration on a reference substrate.

An approximated via inductance (L_{via}) was then extracted from the reflection data using the following method. The input impedance was assumed to be $Z_L = R + j\omega L_{\text{total}}$, where $\Omega = 2\pi f$. The reflection was converted to the input impedance, the imaginary part of which was plotted against frequency, and the total inductance (L_{total}) was obtained from the fitted slope. The simplified equivalent circuit for the measurement and via inductance extraction is shown in Figure 18. This simple approach usually provided a good fit up to approximately 30 GHz.

The value of a single via was finally obtained by assuming that the total inductance was the sum of a single via down and two return vias in parallel (i.e., the contribution of the straps and any mutual inductances were neglected):

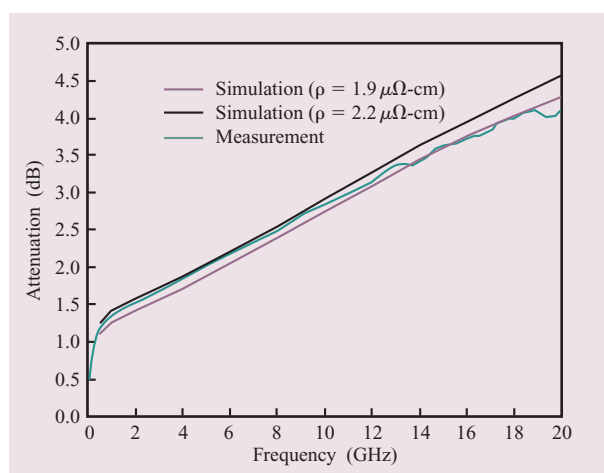


Figure 17

Measured and simulated attenuation per unit length for differential microstrips. Simulations were performed using the IE3D** software tool from Zeland Software, Inc. [53]. IE3D is a method-of-moments-based electromagnetic field simulator.

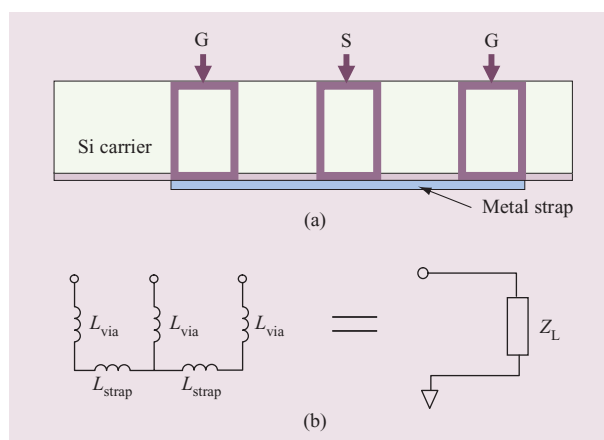


Figure 18

(a) Cross section and probing configuration of strapped through-vias with ground-signal-ground connected by a metal strap. (b) An equivalent circuit used to extract via inductance.

$$L_{\text{total}} = L_{\text{via}} + 1/2L_{\text{via}},$$

and therefore

$$L_{\text{via}} = 2/3L_{\text{total}}.$$

Measurements were taken at several locations on two wafers of different thicknesses. Within each wafer the measured values for total inductance were very uniform, as shown in Figure 19. The slight spread between the

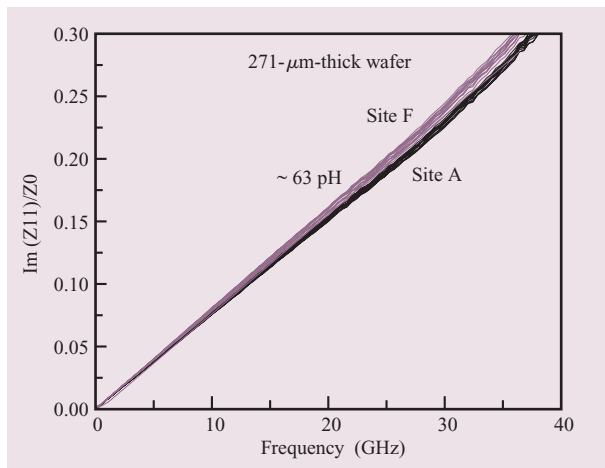


Figure 19

Measured total inductances of through-via sites on 271-μm-thick wafer.

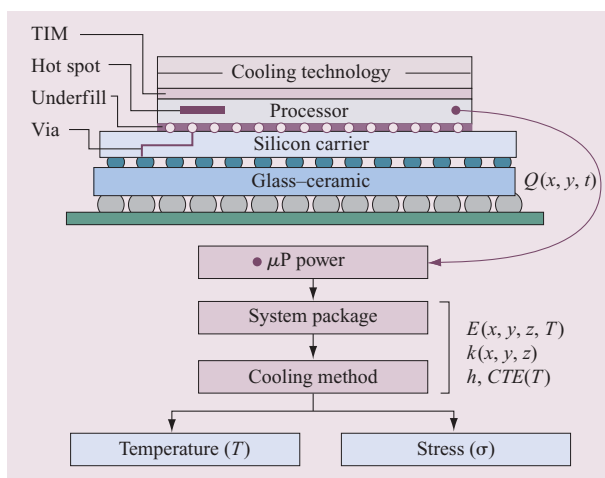


Figure 20

Elements of an SOP for FEM modeling. (Q = volumetric density increase from heat; E = Young's modulus; k = thermal conductivity; h = thermal heat flux; TIM = thermal insulation material.)

curves is due to the strap size (larger strap sizes correlate with lower total inductance). The spread is small enough to justify neglecting the L_{strap} term in the via inductance extraction.

In summary, values of 27 pH and 42 pH were respectively found for a 185-μm-thick wafer and a 271-μm-thick wafer, resulting in approximately 0.15 pH/μm for a single via inductance of that specific diameter and pitch. These values compare well with previous work. Wu et al. [56] showed 107 pH for a 170-μm-thick wafer, or

0.63 pH/μm, with a narrower via (16-μm diameter). These relatively low through-via inductances are important for low-distortion signal interconnects and low-inductance power-delivery networks.

Electrical characterization conclusions

This section has shown the electrical performance characterization of coplanar waveguides, differential microstrips, and through-vias. It was pointed out that 1-mm-long CPWs support a 9-GHz bandwidth, which is adequate for applications with low- to mid-range data rates, while the differential microstrips achieved a 20-GHz bandwidth over 7 mm, which is appropriate for high-data-rate applications. Because of the lower resistive losses and much lower crosstalk on such interconnections than on chip, the silicon carrier can offer much higher bandwidth than BEOL wiring while providing a higher density of wiring than package interconnects with crosstalk of no greater magnitude. Frequency domain measurements of strapped through-vias were performed, and an effective via inductance of 0.15 pH/μm for a 100-μm pitch was extracted using a simple equivalent circuit model. This low inductance is important for low-distortion signal interconnects and low-inductance power-delivery networks.

Thermomechanical modeling, simulation, and characterization

Thermomechanical overview

The distribution of thermal and mechanical stress within a multichip package plays an important role in the design and testing of an SOP module. Conventional wisdom states that if the CTE values of constituent materials (such as silicon and its carrier) are well matched, the ensuing thermomechanical stress is correspondingly reduced. This is true, but consideration must also be given to increasing power dissipation in a silicon chip with hot spots generating strongly nonuniform spatial power density, $Q(x, y)$. Thus, the validity of stresses that were caused by such transients or hot spots in operation, power on, and power off should be determined. The effect of steady and transient temperature on the mechanical stress generated within the critical elements of an SOP is therefore considered in a successful design. Within the context of an SOP application, three areas are considered for detailed discussion: the SOP module, μ-C4s, and through-vias.

Figure 20 shows a cross section of an SOP module shown with only a single processor. Transient power dissipated by a processor is denoted by $Q(x, y, t)$. The power generated by the electronic circuits embedded in the active chips as well as in the silicon carrier is eventually removed by a cooling device. An SOP may

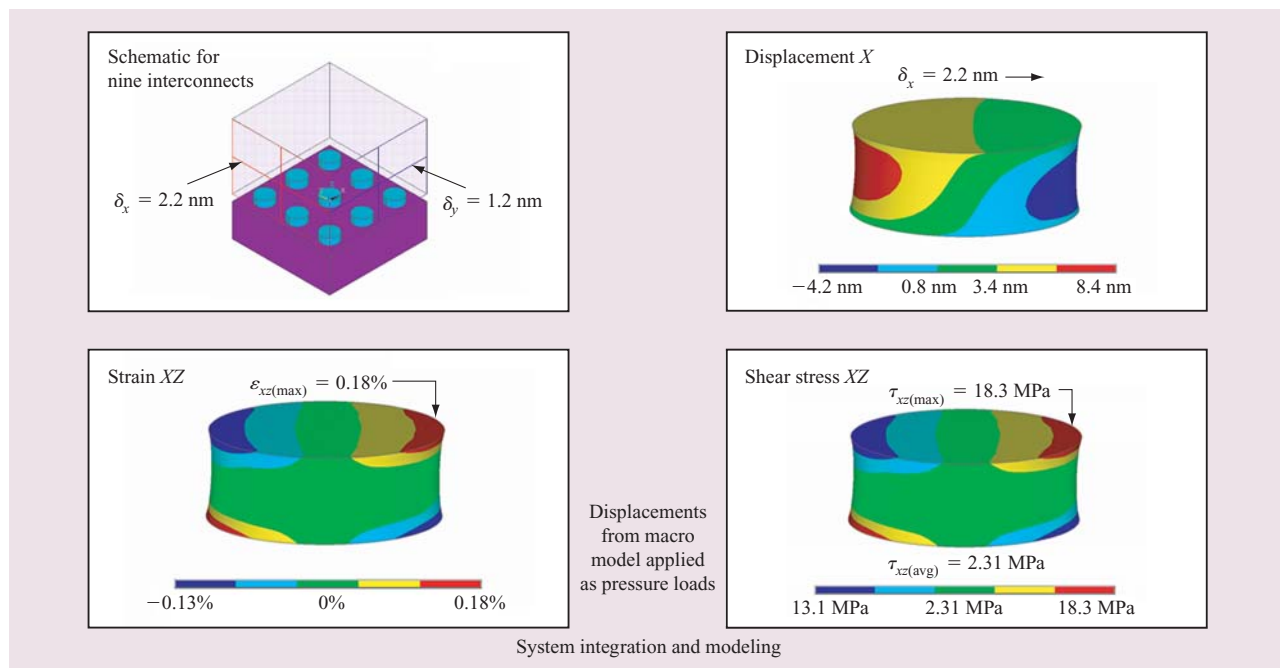


Figure 21

Microbump stress and strain results for $10\text{-}\mu\text{m} \times 25\text{-}\mu\text{m}$ 63Pb37Sn solder interconnection. (Modeling software from ANSYS, Inc. [55].)

actually consist of several silicon-based chips placed on a single silicon carrier. For example, it may comprise processors, memory stacks, and a switch. The chips are attached to a thinned silicon carrier (for example, $300\text{ }\mu\text{m}$ or less than $100\text{-}\mu\text{m}$ thickness) through a densely packed array of $\mu\text{-C4s}$. Hence, the interprocessor communication occurs through the multilayer metallization that connects $\mu\text{-C4s}$ and vias accordingly. The average power dissipation in each chip was considered in addition to hot spots. In addition to average power, the processors can contain hot spots with a power density five times greater than the average.

SOP module

The objective of building a finite element model (FEM) is to estimate the temperature, T , and stress, σ , within the SOP module when it is subjected to a power distribution, $Q(x, y, t)$. A more ambitious goal would be to determine whether the most probable maximum stress within an SOP would ever exceed the failure stress of the corresponding material. The physical properties of the materials (represented by Young's modulus, E , thermal conductivity, k , coefficient of thermal expansion, CTE , etc.) and boundary conditions determine the temperature and stress in a module. A variety of boundary conditions are encountered in a system; for example, the cooling device represents a convective flux defined by its film

heat-transfer coefficient, h , whereas the C4 side of the glass-ceramic represents a conduction-limited semi-insulator. A FEM model must be constructed to capture the effects of all anticipated scenarios without becoming unduly complex.

Stress in $\mu\text{-C4s}$ and mechanical testing

The initial development of a model to increase understanding of stress and strain levels in a $\mu\text{-C4}$ has begun with the use of a macro-micro model. In the finite element model, the macro characteristics of the structure can be considered while still providing the micro-level detailed understanding of the high volumes of each of the small features that is required for an understanding of mechanical characteristics. For example, the model addresses the large quantity of microjoins used in the structure while increasing understanding of the actual stress and strain on an individual $\mu\text{-C4}$ level. **Figure 21** shows this macro model with an example of X displacements made for the $\mu\text{-C4}$ level to show strain in XZ and shear stress in XZ . In this way the relative pressure loads in the macro model can be distributed to the solder interconnections for relative comparison.

The macro- and micro-mechanical modeling of stress in $\mu\text{-C4s}$ can then be evaluated across the various BLM and solder interconnections, as previously discussed in

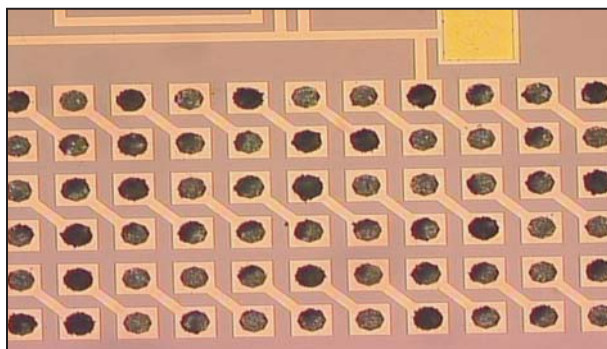


Figure 22

Eutectic microbump mechanical pull test showing 100% solder “taffy pulls” as desired.

the subsection on μ -C4 interconnection development. Comparison of mechanical models and actual sample mechanical testing can then be correlated to optimize suitable structures for a targeted application through the use of mechanical pull and shear tests. Pull-testing results can lead to greater understanding of failure modes.

Figure 22 shows an example of a test structure used in a mechanical pull test of eutectic solder μ -C4s showing 100% failure in solder.

Through-vias

Differential thermal expansion of the via structure during manufacturing processing of the via and inter-level dielectric (ILD) levels is a critical issue in via design. This problem has been examined using 2D axis-symmetric finite-element stress modeling using the ANSYS** [55] modeling package.

Stress and deformation must be evaluated at each stage of the via manufacturing process at the temperature extremes encountered. Elastic properties are characterized by the elastic modulus and Poisson ratio. For some materials such as copper, the yield strength of the material is likely to be exceeded, and the nonlinear properties must be included. A stress-strain curve can be incorporated, but simple yield stress is usually sufficient. The range of temperatures means that the thermal expansion must be included. In addition, shear stresses must be evaluated at material interfaces and compared with the adhesion strengths between materials.

Materials are added sequentially during processing, and not all layers are present at each process step. However, the modeling process is simplified if all of the material layers are included in the initial finite element meshing. This can be accommodated by giving material layers that have not yet been deposited a zero modulus so that they do not contribute any forces to existing layers.

As examples, consider the copper-composite-filled via shown in Figure 9 and the via-last vias shown in Figure 10. **Figure 23** [55] shows the deformation of corresponding finite element cells after deposition of the first BEOL CVD oxide layer on top of the completed via for a 50- μ m by 100- μ m-deep via at maximum and room

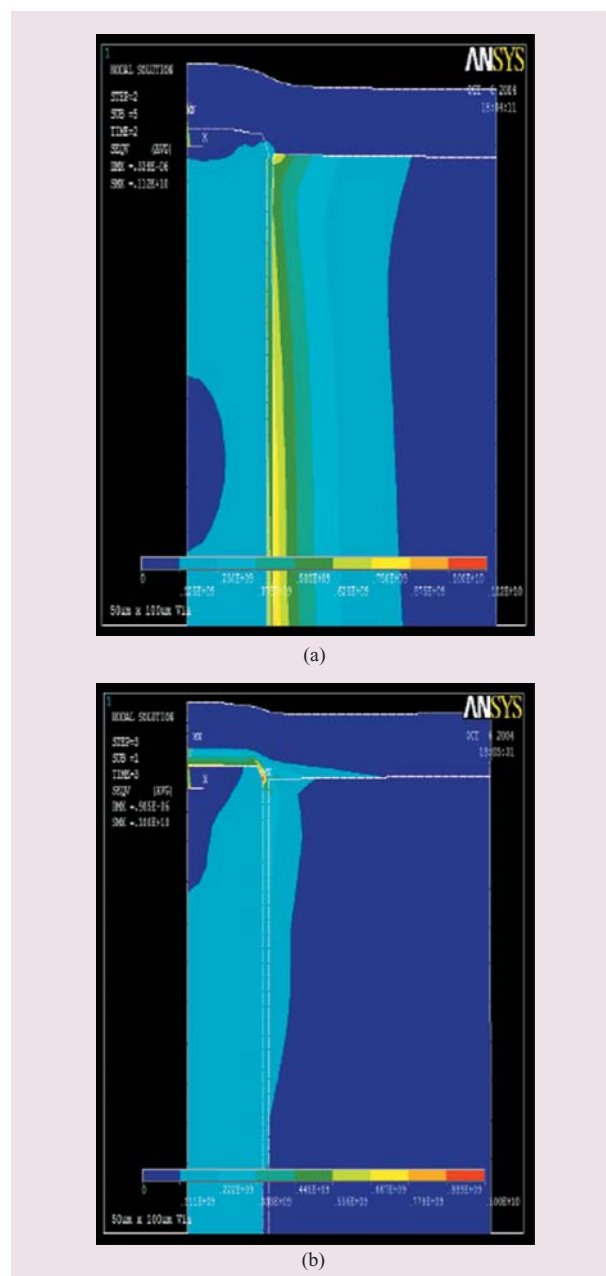


Figure 23

Mechanical modeling for Cu in 50- μ m $\times$ 100- μ m-deep via for (a) 400°C and (b) room temperature, respectively. (Modeling software from ANSYS, Inc. [55].)

temperature. The deformation, defined as the vector deviation of each layer from its nominal starting point, has been exaggerated by a factor of 10 so that it can be better seen.

The highest stress conditions are generally seen at the via to adjacent wiring and dielectric layers. Understanding of the mechanical aspects of via structure and process flow can be leveraged to minimize the maximum vertical stress for use in silicon-based technology. From the understanding of structure and stresses (e.g., for chip stack or SOP, such as electro-optic transceivers or silicon carriers), the electrical and mechanical design specifications for the product application can be satisfied utilizing silicon through-via technology.

Chip stack and SOP assembly, test, and module reliability

A critical element of a chip stack or SOP product is the ability to test, assemble, and ensure module reliability for the product application. The development of SOP technology has included a wide variety of test methods, assembly development, technology demonstrations, and reliability assessments which continue at the time of this publication. This section of the paper discusses some technology challenges and demonstrations with results that help to enable SOP technology. Targeted research to support multiple applications including chip stack (for example with wafer-level processing), single-chip and multichip modules is described. Module reliability for chip stacks with copper-bonded (permanent) interconnections is studied. This differs from chip-to-silicon copper solder (reworkable) interconnections. Thus, depending on structure, interconnect, and application, the assembly and test must support the required product reliability. Technology challenges for assembly, test, and module reliability of SOP structures are summarized in **Table 5**. A discussion of the technical challenges follows.

Assembly methodology depends on a number of factors, including cost, number of chips and components to be packaged, assembly yields, and test methodology. For example, for a single chip on a package or two chips on a package, assembly may be completed after wafer test and prior to full functional test as a methodology to minimize testing cost. For multichip modules with complex chips, each chip would likely be functionally tested prior to assembly and then assembled on the multichip module in order to avoid excessive assembly, test, and rework of the entire multichip module and any specific chips which might be defective or out of acceptable functional specification.

For fabrication, assembly, test, and reliability studies, μ -C4s of four solder compositions and multiple ball-

Table 5 Technology challenges for chip stack or SOP structures.

<i>Technology</i>	<i>Technical challenge</i>
Assembly	Microbump volume/co-planarity
	Pad wetting
	Cleaning
	Assembly yield/rework
Test/burn-in	Area contact
	Contact resistance
	Probe tip/co-planarity
	Known good die testing with microbumps
Reliability	Module reliability stressing
	Electromigration/thermomigration
	Bias testing
	High-temperature storage
	Deep thermal cycling
	Shock and vibration

limiting metallurgies are under investigation. The solder compositions (in wt.%) have included 1) high-lead solder (Pb/Sn; 97/3); 2) eutectic solder (Pb/Sn; 37/63); 3) no-lead solder from the Sn-Ag-Cu family of alloys (>95% Sn + additives); and 4) no-lead solder (Au/Sn; 80/20). The use of lead solders at 100- μ m and 50- μ m pitches permits direct comparison with a larger dataset and years of experience when compared with 200-, 225-, and 250- μ m pitch interconnection using Pb/Sn 97/3 and Pb/Sn 36/63.

For fabrication, The ability to fabricate each solder composition (as given above and discussed in the section on μ -C4 interconnection development) for μ -C4s has been demonstrated using selective plating, injection-molded solder (IMS) technology, and an alternate fabrication process.

Assemblies of hardware have been demonstrated using one or more chips assembled on a package as well as chip-on-chip or wafer-to-wafer-level processing attachment using solder interconnection or copper-to-copper bonding. Initial studies have utilized multiple test vehicles which permit chip-to-Si-carrier attachment with 25- μ m microbumps on a 50- μ m pitch and 50- μ m microbumps on a 100- μ m pitch. Eutectic, Pb-free, high-melt, and AuSn solders have been demonstrated. For eutectic and lead-free solder assemblies, hundreds of joins have been performed, with interconnections on a given test vehicle ranging from 2,160 to more than 10,000 I/Os per die. Taking as representative a die with 5,200 microbumps at 50- μ m pitch, assemblies have been completed with 100% good interconnection. **Figure 24** shows representative microbumps for (a) Pb/Sn eutectic and (b) Pb-free solder with 50- μ m pitch, as well as (c) assembled chips, and (d) a microbump cross section. Assembly studies and characterization of these structures are continuing using

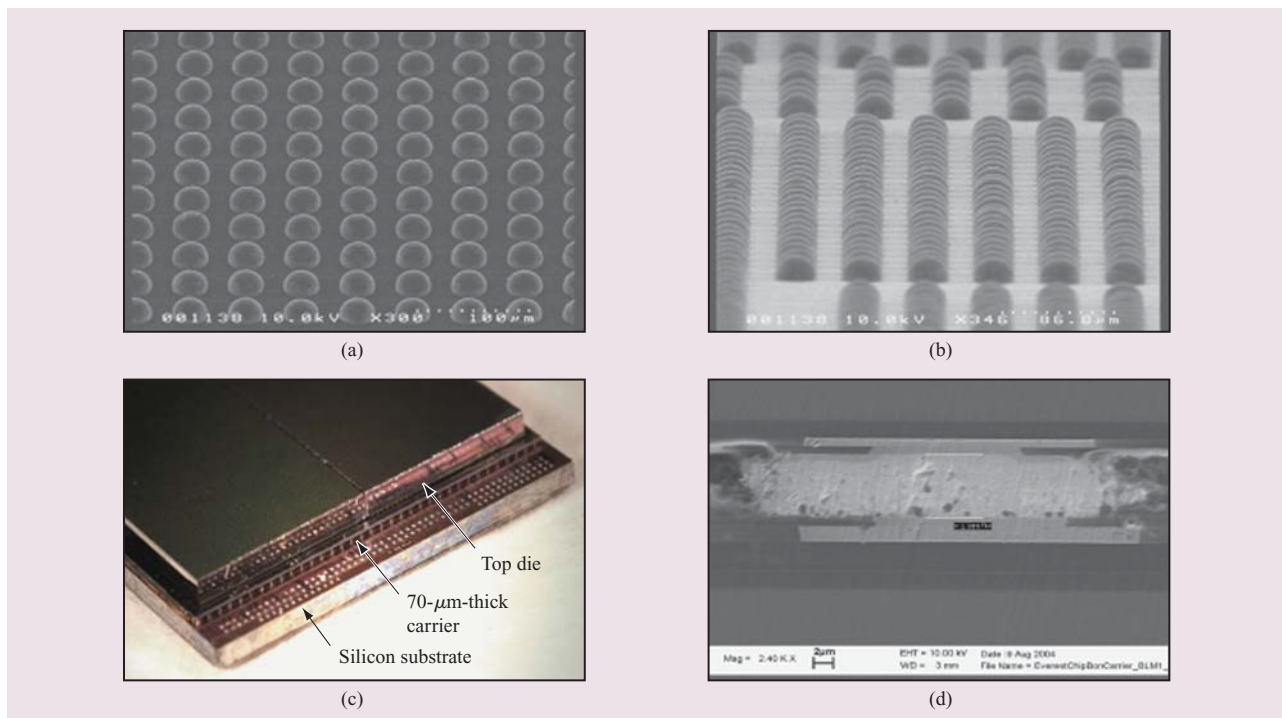


Figure 24

Microbumps in assembly interconnection showing (a) PbSn eutectic assembly; (b) Pb-free solder, with (c) and (d) associated assembly examples.

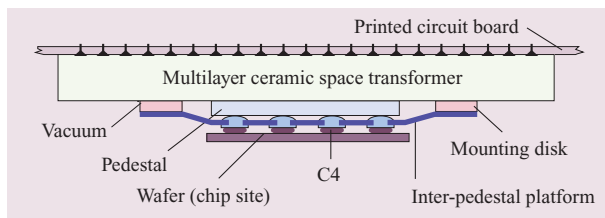


Figure 25

Typical C4 deformation with rigid thin-film interposer (TFI) and compliant Cobra probe.

electrical, mechanical, and reliability stressing. An example of the mechanical testing includes chip pull tests, as shown in Figure 22.

Electrical test method learning for 50- μm -pitch and 100- μm -pitch chip microbumps and SOP interconnections has included investigations using preliminary hand probing, high-speed manufacturing probes, and area array probe testing. Beyond early hand probing, demonstrations of new test chips and test

structures have benefited from IBM manufacturing test using high-speed test probes and area array wafer-testing techniques.

Electrical testing and wafer-testing methodology demonstrations using high-speed manufacturing test probes have provided opens and shorts testing to date. As an example of development, we report on a baseline of current C4 contact probing technologies in IBM and compare them with $\mu\text{-C4s}$ for chips and SOP structures to be tested where new probe technology has been adopted as an integral step to low-cost wafer testing of these advanced structures.

Current wafer testing utilizes a thin-film interposer (TFI) probe to test chips in a wafer at 200- μm pitch, as shown in schematic cross section in **Figure 25**. The probe provides rigid contact and depends on the C4 for compliance; **Figure 26(a)** is a schematic cross section of the TFI probe (left) and the footprint left after contact with a 100- μm solder ball after contact (right). In comparison, **Figure 26(b)** (left) is a schematic diagram of a compliant Cobra** probe, which does not require C4 compliance but does require some surface movement to break through oxides on the C4 surface. Figure 26(b) (right) shows a Cobra-tested C4 solder bump. To scale

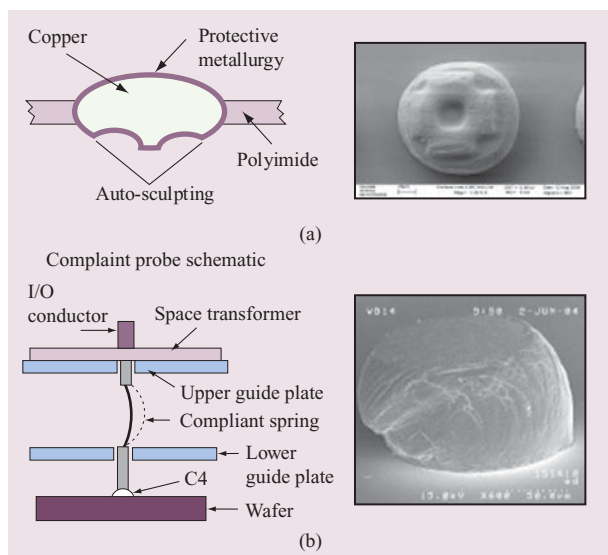


Figure 26

(a) Thin-film interposer (TFI) contact schematic cross section (left) and probed controlled collapse chip connection (C4) right. (b) schematic cross section (left) and probed C4 (right).

current technology from 200- μm pitch to fine-area 50- μm pitch and 100- μm pitch for wafer testing, a new probe platform has been defined, and assessment is underway. The new wafer-testing platform can utilize a scaled-down probe tip where area array fabrication and contact have been demonstrated using area array 50- μm pitch. It is believed that this technology approach can be scaled well below 50- μm pitch. In addition, an assessment with a backup-compliant probe technology has been defined that also has the opportunity to provide wafer testing at 100- μm or 50- μm pitch or less. Investigation and optimization of the new area array test platform and probe tips for area array wafer and die testing are continuing. **Figure 27** shows an early-development 50- μm -pitch $\mu\text{-C4}$ array contact using test probe tips also at 50- μm pitch.

Initial basic electrical measurements include electrical dc contact resistance, pad deformation, and the ability to provide a reliable contact. Using automated four-point resistance probe card testing of the microjoin chains, dc testing of some test structures was performed. A particularly useful microjoin chain macro included a test vehicle design that allows the measurement of a growing sequence of chain links to be precisely measured and plotted. Using these chains, as well as independent three-point measurements of individual microjoins, a measured resistance of $\sim 20\text{ m}\Omega$ for the 50- μm -diameter bumps and $\sim 50\text{ m}\Omega$ for the 20- μm -diameter bumps was obtained (**Figure 28**).

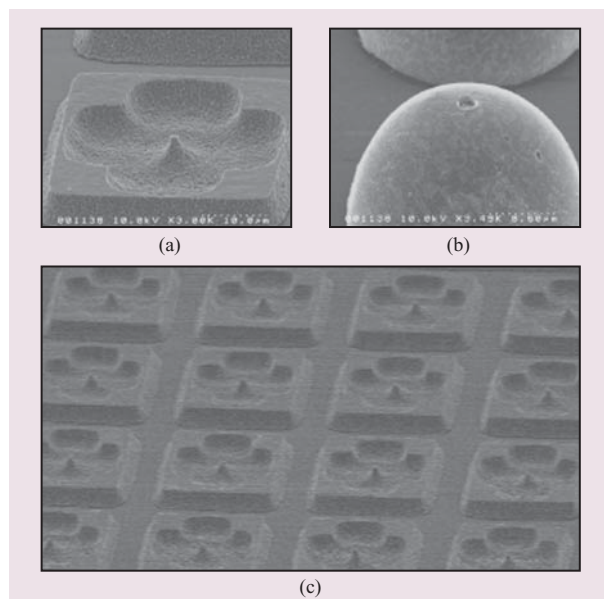


Figure 27

(a) Single probe tip, (b) tested microbump, and (c) area array pitch probe tip array shown for area array electrical testing at 50 μm .

Reliability testing for silicon structures with silicon through-vias, coplanar waveguides built using BEOL processing, $\mu\text{-C4s}$, and module structures has been defined, and initial learning has begun. JEDEC-compatible stress testing [57] has included focus on deep-thermal-cycle stress testing from -55°C to 125°C , temperature and humidity bias testing, electromigration stressing, thermal migration stress testing, high-temperature storage, power cycling, and shock and vibration testing.

Reliability test results for $\mu\text{-C4s}$ of 50- μm size on 100- μm pitch included passing 1,000 deep temperature cycles (DTCs) of -55°C to $+125^\circ\text{C}$ and 1,500 thermal cycles of 0°C to 100°C . Electrical resistance was measured to increase ranging from 3.5% to 9.5% for the DTC samples.

For 25- μm solder bumps on 50- μm pitch, reliability test results showed the following: Non-underfilled samples survived 2,000 cycles of deep thermal cycling from -50°C to $+125^\circ\text{C}$. Electromigration testing showed that samples survived temperatures of 150°C at 62 mA per connection for 2,000 hours and 100 mA per connection for more than 920 hours, respectively. Temperature and humidity with bias voltage testing survived 500 hours without underfill at 1.5 V.

Electrical, mechanical, and physical analysis results from reliability stress testing are being used to provide understanding and improvement in structure and testing methods as research continues.

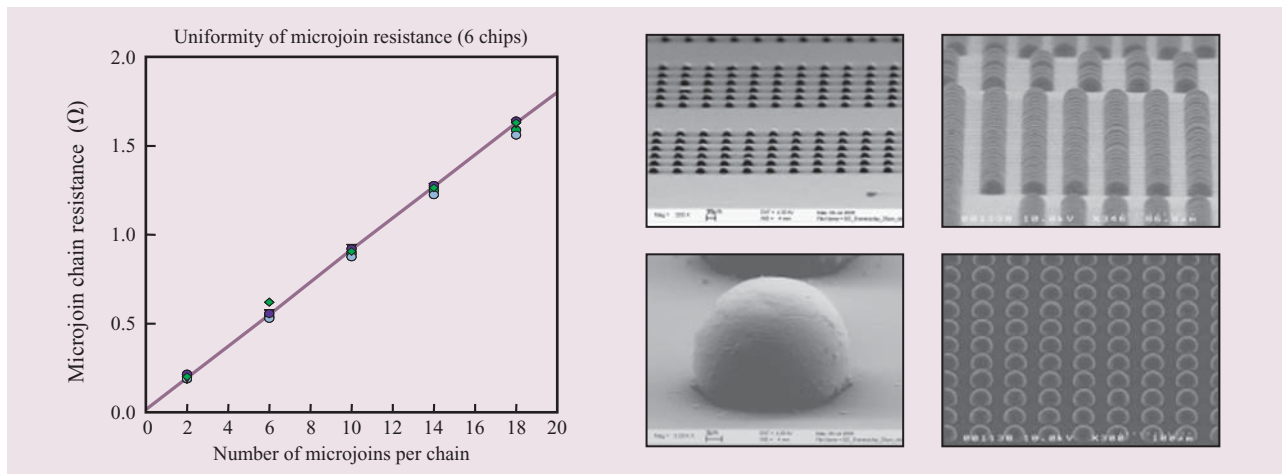


Figure 28

50- μm bumps on 100- μm -pitch microbumps with 20-m Ω resistance per bump and 20- μm -diameter microbumps on 50- μm pitch showing examples of microbump arrays and microjoin resistance measurements.

Summary

In summary, a next-generation system-on-package (SOP) technology continues to be explored at IBM, utilizing newly developed silicon through-via conductors, semiconductor BEOL multilevel wiring, and fine-pitch I/O interconnection for three-dimensional integration of this technology for a variety of applications. The new structures have been electrically designed, modeled, and characterized to provide high-speed interconnection and high bandwidth with I/O and wiring densities that are ten to a hundred times denser than current industry structures. Mechanical modeling, assembly, test, and reliability learning have continued to indicate that this new technology can be achieved and may support a broad range of SOP applications.

The technology appears to be able to scale with technology roadmap needs for electrical, thermal, and I/O scaling for semiconductor advances. Continued technology-based research and development will help to define a database for preferred structures and best manufacturing processes, including silicon package fabrication, test, and assembly. It will also help direct the technology to product applications which show the most cost-competitive product offerings.

Future work on SOP technology will include the assessment of silicon through-via conductors, electrical characterization of structures, opto-electrical characterization, and mechanical and reliability assessments. Future work will also include passive component and active circuit integration for advanced three-dimensional structures. Silicon and packaging integration using new 2D and 3D structures are of

interest to support system requirements and new volume-based product applications.

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